USER MANUAL

PA-J501

15.6" High Performance
POS Terminal

PA-J501 M2

PA-J501 15.6” High Performance POS Terminal

DISCLAIMER

This user’s manual is meant to assist users in installing and setting up the system. The information contained in this document is subject to change without any notice.

CE NOTICE

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC NOTICE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

You are cautioned that any change or modifications to the equipment not expressly approve by the party responsible for compliance could void your authority to operate such equipment.

	**CAUTION:** Danger of explosion may occur when the battery is incorrectly replaced. Replace the battery only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

	**WARNING:** Some internal parts of the system may have high electrical voltage. We strongly recommend that only qualified engineers are allowed to service and disassemble the system. If any damages should occur on the system and are caused by unauthorized servicing, it will not be covered by the product warranty.

Contents

Revision History

The revision history of PA-J501 User Manual is described below:

Version No.	Revision History	Date
M2	The description of Section 3.5.12 Cash Drawer Port (DRW) has been revised. (Page 3-16)	2023/04/25
M1	Initial Release	2022/7/11

1 Introduction

This chapter provides the introduction for PA-J501 system as well as the framework of the user manual.

The following topic is included:

- About This Manual

1.1 About This Manual

Thank you for purchasing our PA-J501 system. The PA-J501 is an updated system designed to be comparable with the highest performance of IBM AT personal computers. The PA-J501 provides faster processing speed, greater expandability and can handle more tasks than before. This manual is designed to assist you how to install and set up the whole system. It contains 5 chapters and 2 appendixes. Users can configure the system according to their own needs. This user manual is intended for service personnel with strong hardware background. It is not intended for general users.

The following section describes the structure of this user manual.

Chapter 1 Introduction
This chapter introduces the framework of this user manual.

Chapter 2 Getting Started
This chapter describes the package contents and system specifications, and illustrates the physical appearances for PA-J501 system. Read the safety reminders carefully on how to take care of your system properly.

Chapter 3 System Configuration
This chapter describes the locations and functions of the system main board components. You will learn how to properly configure the connectors and system configuration jumpers on the main board and configure the system to meet your own needs.

Chapter 4 Software Utilities
This chapter introduces how to install Intel Chipset Software Installation Utility, Graphics Driver Utility, Intel Management Engine Components Installer Driver Utility, LAN Driver Utility, Serial IO Driver Utility and Sound Driver Utility.

Chapter 5 BIOS Setup
This chapter provides BIOS setup information.

Appendix A System Diagrams
This appendix provides the exploded diagrams and part numbers of PA-J501.

Appendix B Technical Summary
This appendix provides the information about the system block diagram, allocation maps for system resources, Watchdog Timer Configuration and Flash BIOS Update.

2 Getting Started

This chapter provides the introduction for the PA-J501 system as well as the framework of the user manual.

The following topic is included:

- About This Manual
- POS System Illustration
- System Specifications
- Safety precautions

Experienced users can jump to Chapter 3 on page 3-1 for a quick start.

2.1 Package List

If you discover any of the items listed below are damaged or lost, please contact your local distributor immediately.

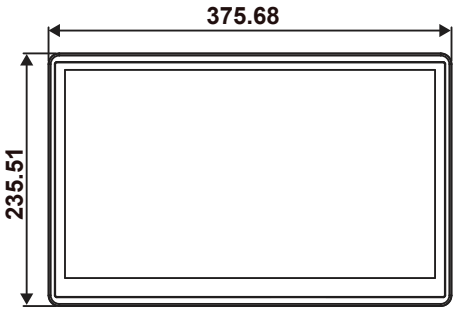
Item	Q'ty
PA-J501 POS System	1
Manual / Driver DVD	1

2.2 System Overview

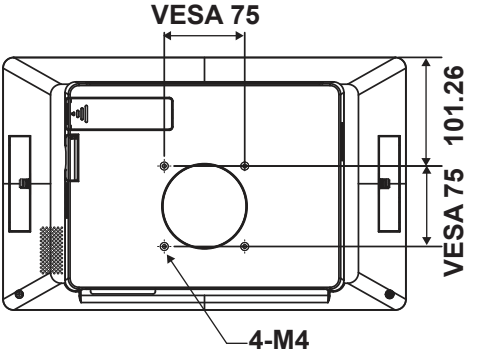
Unit: mm

2.2.1 Panel PC

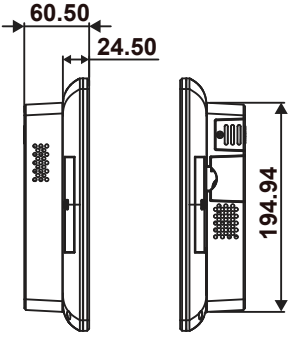
Front View



Rear View



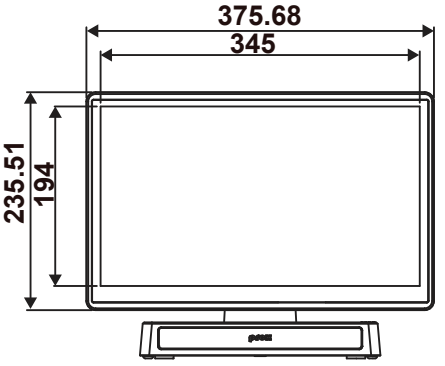
Side View



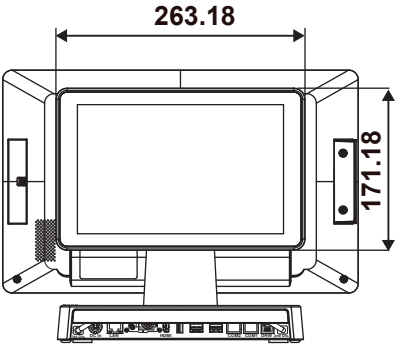
2.2.2 Normal Stand Only

Unit: mm

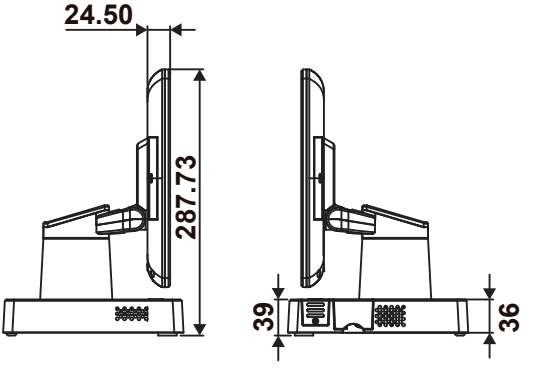
Front View



Rear View



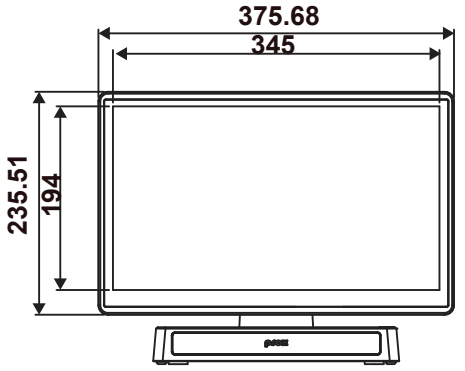
Side View



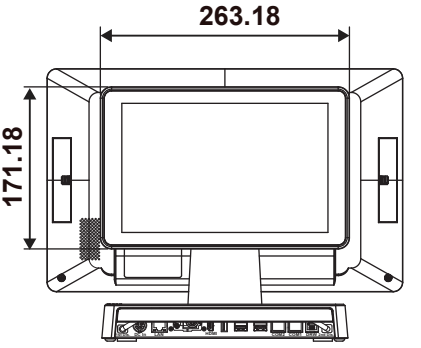
2.2.3 Normal Stand with 10.1" 2nd Display

Unit: mm

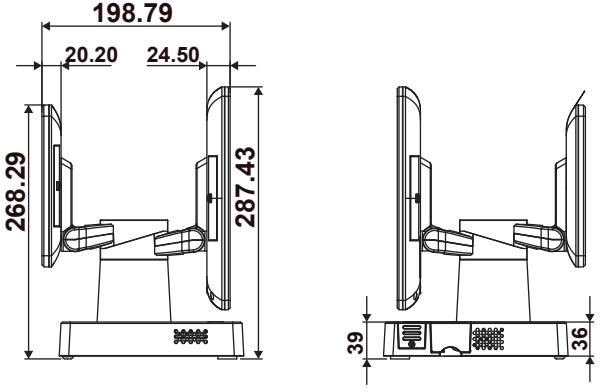
Front View



Rear View



Side View



2.3 System Specifications

System	
CPU Support	➢ Intel® Celeron® J6412 (fanless)
Memory	➢ 1 x DDR4 260-pin SO-DIMM slot (up to 16GB)
Network	➢ 1 x RJ45, 10/ 100/1000 Mbps ➢ 1 x M.2 (Key E, 2230)
Storage	➢ 1 x M.2 2242 / 1 x M.2 2280
Audio	➢ 1 x 2W speaker
System Weight	➢ **PPC:** 3.6 kg ➢ **POS:** 4.23 kg ➢ **POS + 2nd Display:** 5.33 kg
Dimensions (W x H x D)	➢ **PPC:** 375.68 x 235.51 x 60.5mm ➢ **POS:** 375.68 x 287.43 x 194.95mm ➢ **POS + 2nd Display:** 375.68 x 287.43 x 213.26mm
O.S. Support	➢ Windows 10, Windows 11
Storage	
SATA	➢ 1 x M.2 2242 / 1 x M.2 2280, SATA interface
I/O Ports	
Display	➢ 1 x Mini DP for Primary display (for Protech original display only) ➢ 1 x Mini DP for 2nd display (for Protech original display only) ➢ 1 x HDMI 1.4
USB	➢ **Rear I/O:** 3 x USB 2.0 / 2 x USB 3.1 ➢ **Side I/O:** USB 2.0
Serial Ports	➢ 2 x RJ45 (all support 5V/12V selectable under BIOS) (RS-232 interface)
LAN	➢ 1 x 2.5G LAN (RJ45)
Cash Drawer	➢ 1 x RJ11 (+12V or +24V selectable) (default at +24V)
DC In	➢ 1 x 4-pin DC power jack (4pin, DIN)
Option	➢ 1 x USB 2.0 or 1 x 24V Power USB (1A) or 1 x DC Out (1A) or 1 x RJ-45 (RS232 interface)

Add-ons	
Customer Display	➢ VFD kit, 20 columns x 2 lines STN LCD display
MSR	➢ JIS I,II, ISO Track1+2+3 (USB interface)
2nd Display	➢ 10.1” with P-cap touch
Fingerprint	➢ Silicon Fingerprint Module (USB interface)
iButton	➢ iButton module (USB interface)
Scanner	➢ **2D:** PDF417, QR Code, Micro QR, Data Matrix
Display	
Primary Display	➢ 15.6”, TFT LCD (Resolution: 1366 x 768) ➢ Brightness: 220 cd/m²
Touchscreen	➢ Bezel-free P-CAP touch panel (USB interface)
2nd Display	➢ 10.1” Monitor with Touch
Environment	
EMC & Safety	➢ CE / FCC
Operating Temp.	➢ 0°C ~ 35°C (32°F ~ 95°F)
Storage Temp.	➢ -5°C ~ 60°C (23°F ~ 140°F)
Humidity	➢ 20% ~ 90%

2.4 Safety Precautions

Before operating this system, read the following information carefully to protect your systems from damages, and extend the life cycle of the system.

1. Check the Line Voltage
   - The operating voltage for the power supply should be within the range of 100V to 240V AC; otherwise, the system may be damaged.

2. Environmental Conditions
   - Place your PA-J501 on a sturdy, level surface. Be sure to allow enough space around the system to have easy access needs.
   - Avoid installing your PA-J501 system in extremely hot or cold places.
   - Avoid direct sunlight exposure for a long period of time (for example, in a closed car in summer time. Also avoid the system from any heating device.). Or do not use PA-J501 when it has been left outdoors in a cold winter day.
   - Bear in mind that the operating ambient temperature is between 0°C and 35°C (32°F and 95°F).
   - Avoid moving the system rapidly from a hot place to a cold place, and vice versa, because condensation may occur inside the system.
   - Protect your PA-J501 from strong vibrations which may cause hard disk failure.
   - Do not place the system too close to any radio-active device. Radio-active device may cause signal interference.
   - Always shut down the operating system before turning off the power.

3. Handling
   - Avoid placing heavy objects on the top of the system.
   - Do not turn the system upside down. This may cause the hard drive to malfunction.
   - Do not allow any objects to fall into this device.
   - If water or other liquid spills into the device, unplug the power cord immediately.

3 System Configuration

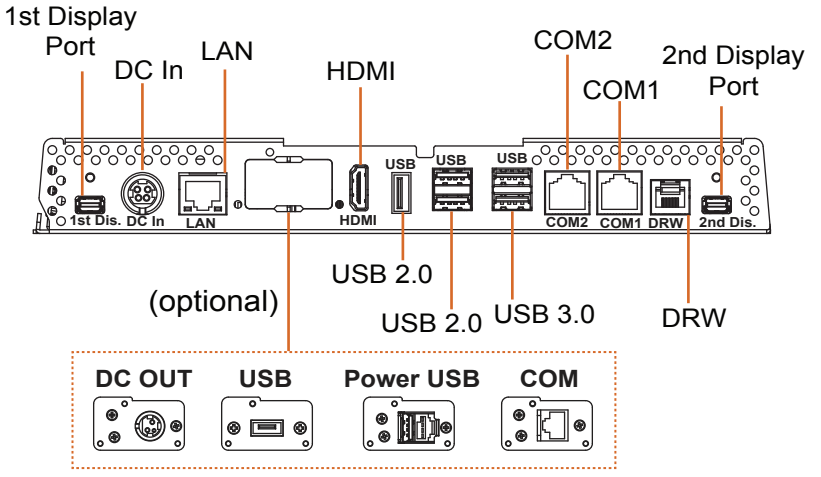
This chapter provides the information for the PA-J501 system. It describes the jumper and connector settings, component locations, and pin assignment.

The following topics are included:

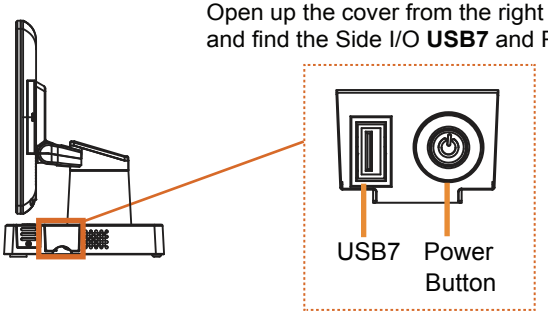
- System External I/O Port Diagram
- Mainboard Component Locations & Jumper Setting
- How to Set Jumpers
- Setting Connectors and Jumpers

3.1 System External I/O Ports Diagram

Rear I/O

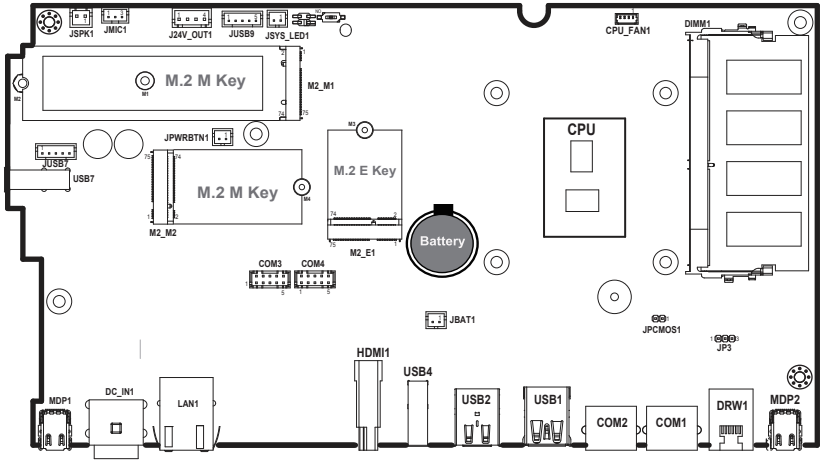


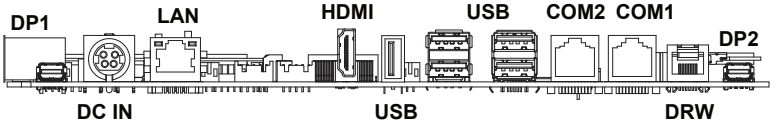
Side I/O



3.2 Mainboard Component Locations & Jumper Setting

M/B: PB-J501



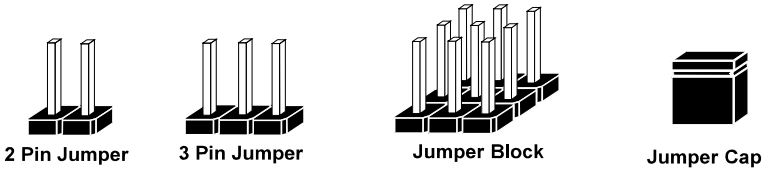


3.3 How to Set Jumpers

You can configure your board by setting the jumpers. A jumper consists of two or three metal pins with a plastic base mounted on the card, and by using a small plastic "cap", also known as the jumper cap (with a metal contact inside), you are able to connect the pins. So you can set-up your hardware configuration by "opening" or "closing" pins.

Jumpers can be combined into sets that called jumper blocks. When jumpers are all in the block, you have to put them together to set up the hardware configuration. The figure below shows what this looks like.

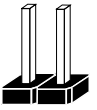
Jumpers & Caps



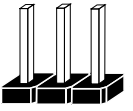
If a jumper has three pins, for example, labeled PIN1, PIN2 and PIN3. You can connect PIN1 and PIN2 to create one setting and shorting. You can also select to connect PIN2 and PIN3 to create another setting. The same jumper diagrams are applied all through this manual. The figure below shows what the manual diagrams look and what they represent.

Jumper diagrams

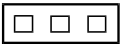
Jumper Cap looks like this

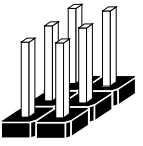


2 pin Jumper looks like this

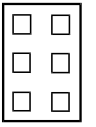


3 pin Jumper looks like this



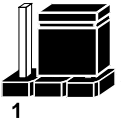


Jumper Block looks like this

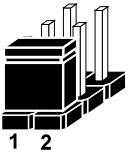


Jumper settings

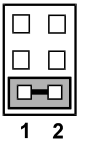
2 pin Jumper closed(enabled)
looks like this



3 pin Jumper
2-3 pin closed(enabled)
looks like this



Jumper Block
1-2 pin closed(enabled)
looks like this



3.4 Main Board Connector & Jumper Quick Reference Table

JUMPER	NAME
Clear CMOS Data Selection	JCMOS1
Cash Drawer Voltage Selection	JP3

CONNECTOR	NAME
DC In Connector	DC In
1st Display Port	MDP1
COM Port RS-232 Connector	COM1, COM2
COM Connector	COM3, COM4
LAN Port Connector	LAN1
USB 2.0 Port	USB4
Dual USB 3.0 Ports	USB1
Dual USB 2.0 Ports	USB2
2nd Display Port	MDP2
HDMI Port Connector	HDMI1
Cash Drawer Port Connector	DRW
Internal USB Wafer	JUSB9
Internal USB Wafer	JUSB7 (co-lay with side I/O USB7)
Speaker Wafer	JSPK1
Microphone Connector	JMIC1
Power Output 24V Wafer	24V_OUT1
System LED Wafer	JSYS_LED1
CPU FAN Wafer	CPU_FAN1
Power Button Wafer	JPWRBTN1
Battery Wafer	JBAT1
System Reset Wafer	JRST1
M.2 M-Key Connector for SSD	M2_M1, M2_M2
M.2 E-Key Connector for Wi-Fi	M2_E1

3.5 Setting Main Board Connectors and Jumpers

3.5.1 Power Switch

Connector Location: Power Switch

Description: To turn on the system, open up the cover from the right side of PA-J501 Box and press the power switch briefly.

ACTION	ASSIGNMENT
Click	0V
Release	+3.3V

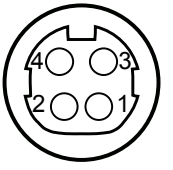
Power Switch

3.5.2 DC IN Connector (DC In)

Connector Location: DC In

Description: Power In Connector

PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	GND	2	GND
3	V24P0A_IN	4	V24P0A_IN



DC In

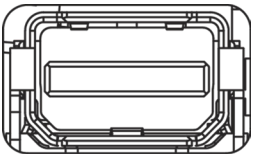
3.5.3 1st Display Port (MDP1)

Connector Location: MDP1

Description: 1st Display Port

Proprietary Pin Assignment for Protech Original Display Only:

PIN	ASSIGNMENT
1	GND
2	EDP_HPD_C_A
3	DDIA_LANE0_DP_C
4	EDP_BKLT_EN_R
5	DDIA_LANE0_DN_C
6	EDP_BKLT_CTRL_R
7	GND
8	EDP_VDD_EN_R
9	DDIA_LANE1_DP_C
10	USB2_P3_DN_C
11	DDIA_LANE1_DN_C
12	USB2_P3_DP_C
13	HD_GND
14	GND
15	LINE-OUT-R
16	DDIA_AUX_DP_C
17	LINE-OUT-L
18	DDIA_AUX_DN_C
19	HD_GND
20	V24P0



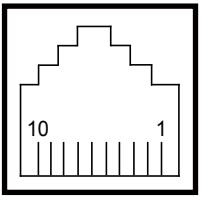
MDP1

3.5.4 COM Ports (COM1, COM2)

Connector Location: COM1, COM2

Description: COM Ports, RJ11

PIN	ASSIGNMENT
1	COM1/2_DCDJ_I
2	COM1/2_RX_I
3	COM1/2_TX_I
4	COM1/2_DTRJ_I
5	GND
6	COM1/2_DSRJ_I
7	COM1/2_RTSJ_I
8	COM1/2_CTSJ_I
9	COM1/2_RI_SEL
10	-



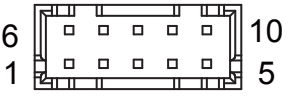
COM1 / COM2

3.5.5 COM Connector (COM3, COM4)

Connector Location: COM3, COM4

Description: COM Ports, COM4 fixed as RS-232

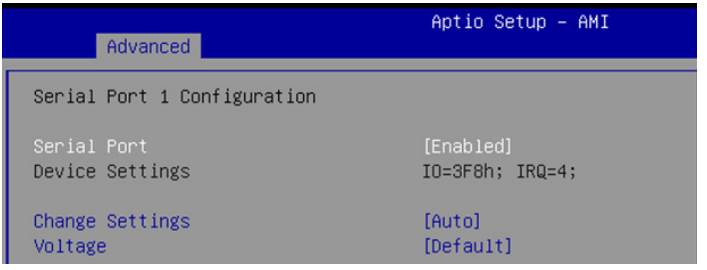
PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	DCD#	5	DSR#
2	RX	6	RTS#
3	TX	7	CTS#
4	DTR#	8	RI#
5	GND	-	



COM3 / COM4

COM1, COM2, COM3 Voltage Adjustment

The voltage of external ports "COM1, COM2 and COM3 (optional) " is made to control on BIOS for your convenience.



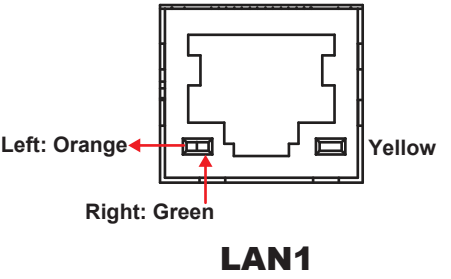
Please refer to the descriptions of **Serial Port 1**, **Serial Port 2 and Serial Port 3 Configuration** under **Advanced > F81967 Super IO Configuration** menu in Chapter 5 BIOS Setup.

3.5.6 LAN Port (LAN1)

Connector Location: LAN1

Description: LAN Port, RJ45

PIN	ASSIGNMENT
R2	LAN1_MDI0_DP
R3	LAN1_MDI0_DN
R4	LAN1_MDI1_DP
R5	LAN1_MDI1_DN
R6	LAN1_MDI2_DP
R7	LAN1_MDI2_DN
R8	LAN1_MDI3_DP
R9	LAN1_MDI3_DN



LAN LED Indicator:

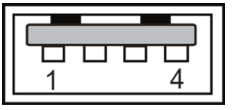
Orange Color Blinking	1G Giga LAN Message Active
Green Color Blinking	2.5G Giga LAN Message Active

Yellow Color On	LAN switch / hub connected.

3.5.7 USB 2.0 Port (USB4)

Connector Location: USB4
Description: USB 2.0 Port

PIN	ASSIGNMENT
1	USB_PW4
2	USB2_P4_DN
3	USB2_P4_DP
4	GND



USB4
(USB 2.0)

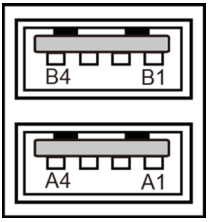
3.5.8 Dual USB 2.0 Ports (USB2)

Connector Location: USB2

Description: USB 2.0 Type A Ports

USB 2.0

PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	USB_PWR8	5	USB_PWR5
2	USB2_P8_DN	6	USB2_P5_DN
3	USB2_P8_DP	7	USB2_P5_DP
4	GND	8	GND



USB2
(USB2.0)

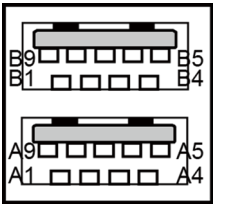
3.5.9 Dual USB 3.0 Ports (USB1)

Connector Location: USB1

Description: USB 3.0 Type A Ports

USB 3.0

PIN	ASSIGNMENT	PIN	ASSIGNMENT
A1	USB_PWR1	B1	USB_PWR2
A2	USB2_P1_DN	B2	USB2_P2_DN
A3	USB2_P1_DP	B3	USB2_P2_DP
A4	GND	B4	GND
A5	USB31_P1_RX_DN	B5	USB31_P2_RX_DN
A6	USB31_P1_RX_DP	B6	USB31_P2_RX_DP
A7	GND	B7	GND
A8	USB31_P1_TX_DN	B8	USB31_P2_TX_DN
A9	USB31_P1_TX_DP	B9	USB31_P2_TX_DP



USB1
(USB3.0)

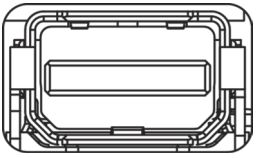
3.5.10 2nd Display Port (MDP2)

Connector Location: MDP2

Description: 2nd Display Port

Proprietary Pin Assignment for Protech Original Display Only:

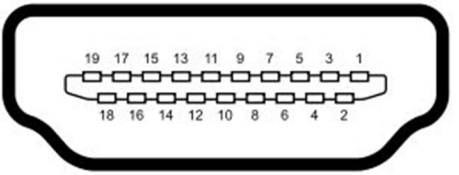
PIN	ASSIGNMENT
1	GND
2	EDP_HPD_C_B
3	DDIB_LANE0_DP_C
4	2ND_BKLT_EN
5	DDIB_LANE0_DN_C
6	2ND_BKLT_CTRL
7	GND
8	2ND_VDD_EN
9	DDIB_LANE1_DP_C
10	USB2_P6_DN_C
11	DDIB_LANE1_DN_C
12	USB2_P6_DP_C
13	GND
14	GND
15	NC
16	DDIB_AUX_DP_C
17	NC
18	DDIB_AUX_DN_C
19	GND
20	V24P0



MDP2

3.5.11 HDMI Port Connector (HDMI1)

Connector Location: HDMI1
Description: Display Port Connector



HDMI1

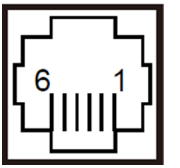
PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	HDMI_P2	2	GND
3	HDMI_N2	4	HDMI_P1
5	GND	6	HDMI_N1
7	HDMI_P0	8	GND
9	HDMI_N0	10	HDMI_CLKP
11	GND	12	HDMI_CLKN
13	GND	14	GND
15	HDMI_SCL_5V	16	HDMI_SDA_5V
17	GND	18	V5P0S_HDM
19	HDMI_HPD	20	-

3.5.12 Cash Drawer Port (DRW)

Connector Location: DRW

Description: DRW is used by default. Adopt the method below:

PIN	ASSIGNMENT
1	COM2_DCDJ_I
2	COM2_RX_I
3	COM2_TX_I
4	COM2_DTRJ_I
5	GND
6	COM2_DSRJ_I



DRW

Cash Drawer CONFIGURATION

The I/O port address of the watchdog timer is 2E (hex) and 2F (hex). 2E (hex) is the address port. 2F (hex) is the data port. User must first assign the address of register by writing address value into address port 2E (hex), then write/read data to/from the assigned register through data port 2F (hex).

SIO Address	
Cash drawer Open	LDN06, 0x81, bit1
Cash drawer Status	LDN06, 0x81, bit0

Configuration Sequence

To program F81967 configuration registers, the following configuration sequence must be followed:

(1) Enter the extended function mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

(2) Configure the configuration registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1). First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required. Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

(3) Exit the extended function mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

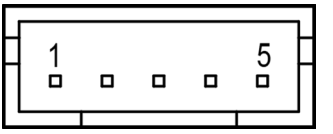
Code example for opening the cash drawer

```
; ------------------------ Enter to extended function mode ------------------------------
mov     dx,     2Eh
mov     al,     87h
out     dx,     al
out     dx,     al
; ---------------------- Select Logical Device 6 of Cash Drawer ---------------------
mov     al,     07h
out     dx,     al
inc     dx
mov     al,     06h
out     dx,     al
;--------------------------------Open the Cash Drawer -----------------------------
mov     al,     81h
out     dx,     al
inc     dx
in      al,     dx
or      al,     02h
out     dx,     al
;--------------------------------Close the Cash Drawer -----------------------------
mov     al,     81h
out     dx,     al
inc     dx
in      al,     dx
and     al,     FDh
out     dx,     al
;--------------------------------Exit the extended function mode -------------------------
dec     dx
mov     al,     AAh
out     dx,     al
```

3.5.13 Internal USB Wafer (JUSB9)

Connector Location: JUSB9

Description: Internal USB Wafer



JUSB9

JUSB9

PIN	ASSIGNMENT
1	USB_PWR9
2	USB2_P9_DN
3	USB2_P9_DP
4	GND
5	GND

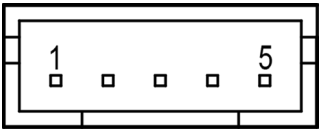
3.5.14 Internal USB Wafer (JUSB7)

Connector Location: JUSB7

Description: Internal USB Wafer (Co-lay with side I/O **USB7**)

JUSB7

PIN	ASSIGNMENT
1	USB_PWR7
2	USB2_P7_DN
3	USB2_P7_DP
4	GND
	GND

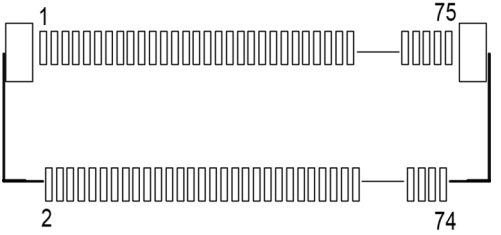


JUSB7

3.5.15 M.2 M-Key Connector for SSD (M2_M1)

Connector Location: M2_M1

Description: M.2 M-Key Connector for SSD



M2_M1

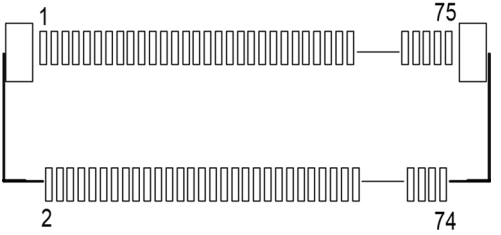
PIN	ASSIGNMENT	PIN	ASSIGNMENT
2	V3P3S_M2_CPU	1	GND
4	V3P3S_M2_CPU	3	GND
6	NC	5	PCIE4_RX_N3
8	NC	7	PCIE4_RX_P3
10	M2_LED1	9	GND
12	V3P3S_M2_CPU	11	PCIE4_TX_N3
14	V3P3S_M2_CPU	13	PCIE4_TX_P3
16	V3P3S_M2_CPU	15	GND
18	V3P3S_M2_CPU	17	PCIE4_RX_N2
20	NC	19	PCIE4_RX_P2
22	NC	21	GND
24	NC	23	PCIE4_TX_N2
26	NC	25	PCIE4_TX_P2
28	NC	27	GND
30	NC	29	PCIE4_RX_N1
32	NC	31	PCIE4_RX_P1
34	NC	33	GND
36	NC	35	PCIE4_TX_N1
38	NC	37	PCIE4_TX_P1
40	NC	39	GND
42	NC	41	PCIE4_RX_N0_SATA1_RXP
44	NC	43	PCIE4_RX_P0_SATA1_RXN
46	NC	45	GND
48	NC	47	PCIE4_TX_N0_SATA1_TXN
50	M2_KEYM_CPU_SSD_RST_R_N	49	PCIE4_TX_P0_SATA1_TXP
52	GPPC_D5_SRCCLKREQ0_N	51	GND
54	WAKE_N	53	CLK_SRC0_DN

PIN	ASSIGNMENT	PIN	ASSIGNMENT
56	NC	55	CLK_SRC0_DP
58	NC	57	GND
60	NC	59	M_KEY
62	NC	61	M_KEY
64	NC	63	M_KEY
66	NC	65	M_KEY
68	NC	67	NC
70	V3P3S_M2_CPU	69	PCIE_SEL
72	V3P3S_M2_CPU	71	GND
74	V3P3S_M2_CPU	73	GND
-	-	75	GND

3.5.16 M.2 M-Key Connector for SSD (M2_M2)

Connector Location: M2_M2

Description: M.2 M-Key Connector for SSD



M2_M1

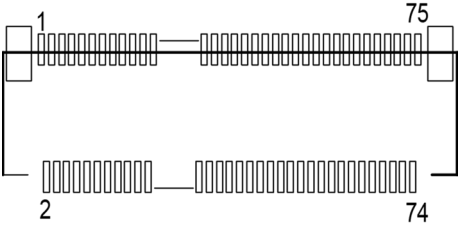
PIN	ASSIGNMENT	PIN	ASSIGNMENT
2	V3P3S_M2_CPU	1	GND
4	V3P3S_M2_CPU	3	GND
6	NC	5	NC
8	NC	7	NC
10	M2_LED2	9	GND
12	V3P3S_M2_CPU	11	NC
14	V3P3S_M2_CPU	13	NC
16	V3P3S_M2_CPU	15	GND
18	V3P3S_M2_CPU	17	NC
20	NC	19	NC
22	NC	21	GND
24	NC	23	NC
26	NC	25	NC
28	NC	27	GND
30	NC	29	PCIE4_RX_N1
32	NC	31	NC
34	NC	33	NC
36	NC	35	NC
38	NC	37	NC
40	NC	39	GND
42	NC	41	SATA_0_RX_DP
44	NC	43	SATA_0_RX_DN
46	NC	45	GND
48	NC	47	SATA_0_TX_DN
50	M2_KEYM_CPU_SSD_RST_R_N	49	SATA_0_TX_DP
52	GPPC_D5_SRCCLKREQ0_N	51	GND
54	WAKE_N	53	CLK_SRC1_DN

PIN	ASSIGNMENT	PIN	ASSIGNMENT
56	NC	55	CLK_SRC1_DP
58	NC	57	GND
60	NC	59	M_KEY
62	NC	61	M_KEY
64	NC	63	M_KEY
66	NC	65	M_KEY
68	NC	67	NC
70	V3P3S_M2_1	69	NC
72	V3P3S_M2_1	71	GND
74	V3P3S_M2_1	73	GND
-	-	75	GND

3.5.17 M.2 E-Key Connector for Wi-Fi (M2_E1)

Connector Location: M2_E1

Description: M.2 E-Key Connector for Wi-Fi



M2_E1

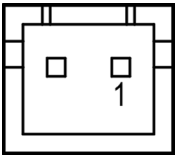
PIN	ASSIGNMENT	PIN	ASSIGNMENT
2	V3.3A_WLAN	1	GND
4	V3.3A_WLAN	3	M_USB2_P10_DP
6	M.2_WLAN_LED1_N	5	M_USB2_P10_DN
8	AVS_I2S2_SCLK_R	7	GND
10	AVS_I2S2_SFRM_R	9	NC
12	AVS_I2S2_RXD_R	11	NC
14	AVS_I2S2_TXD_R	13	GND
16	M.2_BT_LED2_N	15	NC
18	GND	17	NC
20	UART_BT_WAKE_N_R	19	GND
22	SIO_UART0_RXD_R	21	NC
24	E-KEY	23	NC
26	E-KEY	25	E-KEY
28	E-KEY	27	E-KEY
30	E-KEY	29	E-KEY
32	SIO_UART0_TXD_R	31	E-KEY
34	SIO_UART0_CTS_R	33	GND
36	SIO_UART0_RTS_R	35	PCIE3_P10_M2_WLAN_TX_DP
38	NC	37	PCIE3_P10_M2_WLAN_TX_DN
40	NC	39	GND
42	NC	41	PCIE_P4_RXP
44	NC	43	PCIE_P4_RXN
46	NC	45	GND

PIN	ASSIGNMENT	PIN	ASSIGNMENT
48	NC	47	CLK_SRC5_M2_WLAN_DP
50	M.2_BTWIFI_SUS_CLK	49	CLK_SRC5_M2_WLAN_DN
52	M.2_WLAN_PERST_R_N	51	GND
54	BT_RF_KILL_N	53	PCIE_CLKREQ1_N
56	WIFI_RF_KILL_N	55	M.2_WLAN_PE_WAKE_N_R
58	NC	57	GND
60	NC	59	NC
62	NC	61	NC
64	TP	63	GND
66	NC	65	NC
68	NC	67	NC
70	NC	69	GND
72	V3.3A_WLAN	71	NC
74	V3.3A_WLAN	73	NC
-	-	75	GND

3.5.18 Speaker Wafer (JSPK1)

Connector Location: JSPK1
Description: Speaker Wafer

PIN	ASSIGNMENT
1	VOUTP
2	VOUTN

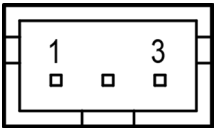


JSPK1

3.5.19 Microphone Connector (JMIC1)

Connector Location: JMIC1
Description: Mic Pin Header

PIN	ASSIGNMENT
1	HD_MIC1-R_L
2	HD_GND
3	HD_MIC1-L_L

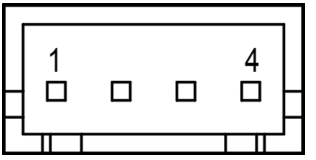


JMIC1

3.5.20 Power Output 24V Wafer (J24V_OUT1)

Connector Location: J24V_OUT1
Description: Power Output 24V Wafer

PIN	ASSIGNMENT
1	24V
2	24V
3	GND
4	GND



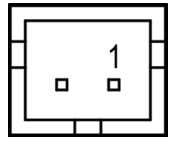
J24V_OUT1

3.5.21 System LED Wafer (JSYS_LED1)

Connector Location: JSYS_LED1

Description: System LED Wafer

PIN	ASSIGNMENT
1	V5P0
2	GND



JSYS_LED1

3.5.22 CPU Fan Wafer (CPU_FAN1)

Connector Location: CPU_FAN1

Description: CPU Fan Wafer

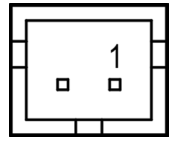
PIN	ASSIGNMENT
1	GND
2	V12P0
3	sense
4	Control

CPU_FAN1

3.5.23 Power Button Wafer (JPWRBTN1)

Connector Location: JPWRBTN1
Description: Power Button Wafer

PIN	ASSIGNMENT
1	V3P3A
2	GND

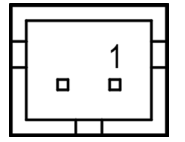


JPWRBTN1

3.5.24 Battery Wafer (JBAT1)

Connector Location: JBAT1
Description: Battery Wafer

PIN	ASSIGNMENT
1	VRTC_BATT
2	GND

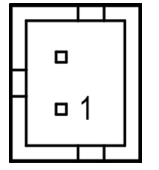


JBAT1

3.5.25 System Reset Wafer (JRST1)

Connector Location: JRST1
Description: System Reset Wafer

PIN	ASSIGNMENT
1	RST_SW
2	GND

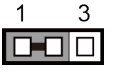
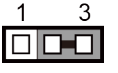


JRST1

3.5.26 Cash Drawer Voltage Selection (JP3)

Jumper Location: JP3

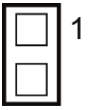
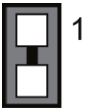
Description: Cash Drawer Voltage Selection

SELECTION	JUMPER SETTING	JUMPER ILLUSTRATION
24V	**1-2** *(Default Setting)*	 **JP3**
12V	2-3	 **JP3**

3.5.27 Clear CMOS Data Selection (JCMOS1)

Jumper Location: JCMOS1

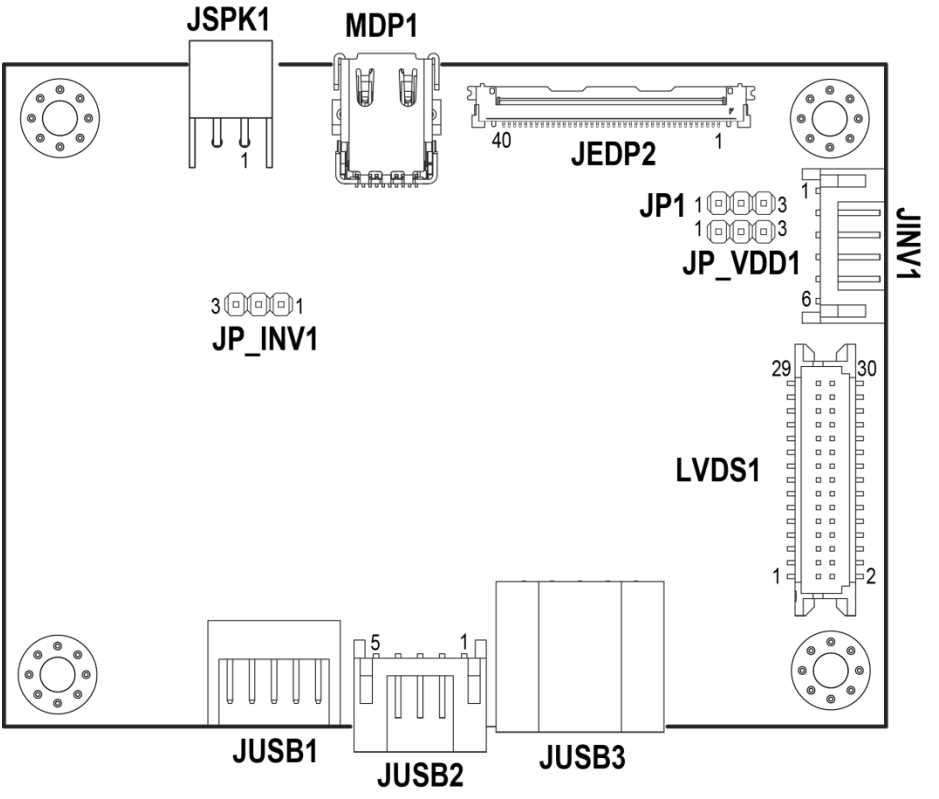
Description: Clear CMOS data selection

SELECTION	JUMPER SETTING	JUMPER ILLUSTRATION
Normal	**Open** *(Default Setting)*	 **JCMOS1**
Clear CMOS Data	1-2	 **JCMOS1**

Note: To clear CMOS data, you must power off the computer and set the jumper to "Clear CMOS" as illustrated above. After five to six seconds, set the jumper back to "Normal" and power on the computer.

3.6 A/D Board Component Locations & Jumper Setting

A/D Board: PR-J500



3.7 A/D Board Connector & Jumper Quick Reference Table

JUMPER	NAME
Backlight Voltage Selection	JP_INV1
LVDS Panel Voltage Selection	JP_VDD1
LVDS Backlight Control	JP1

CONNECTOR	NAME
1st Display Port Connector	MDP1
Embedded DisplayPort Connector	JEDP2
Speaker Connector	JSPK1
Inverter Connector	JINV1
LVDS Connector	LVDS1
USB 2.0 Connector	JUSB1, JUSB2, JUSB3

3.8 Setting A/D Board Connectors and Jumpers

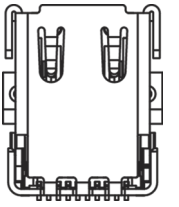
3.8.1 1st Display Port Connector (MDP1)

Connector Location: MDP1

Description: 1st Display Port Connector

Proprietary Pin Assignment for Protech Original Display Only:

PIN	ASSIGNMENT
1	GND
2	EDP_HPD_C_A
3	DDIA_LANE0_DP_C
4	EDP_BKLT_EN_R
5	DDIA_LANE0_DN_C
6	EDP_BKLT_CTRL_R
7	GND
8	EDP_VDD_EN_R
9	DDIA_LANE1_DP_C
10	USB2_P3_DN_C
11	DDIA_LANE1_DN_C
12	USB2_P3_DP_C
13	HD_GND
14	GND
15	LINE-OUT-R
16	DDIA_AUX_DP_C
17	LINE-OUT-L
18	DDIA_AUX_DN_C
19	HD_GND
20	V24P0

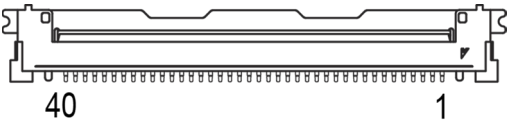


MDP1

3.8.2 Embedded DisplayPort Connector (JEDP2)

Connector Location: JEDP2

Description: Embedded DisplayPort Connector



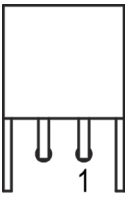
JEDP2

PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	NC	21	LVDS_VDD
2	GND	22	EDP_SELF_TEST
3	NC	23	GND
4	NC	24	GND
5	GND	25	GND
6	NC	26	GND
7	NC	27	EDP_HPD
8	NGND	28	GND
9	EDP_LANE1_DN_C	29	GND
10	EDP_LANE1_DP_C	30	GND
11	GND	31	GND
12	EDP_LANE0_DN_C	32	EDP_BKLT_EN
13	EDP_LANE0_DP_C	33	DP_BKLT_CTRL
14	GND	34	EDP_DCR_EN
15	EDP_AUX_DN_C	35	NC
16	EDP_AUX_DP_C	36	INV_VCC
17	GND	37	INV_VCC
18	LVDS_VDD	38	INV_VCC
19	LVDS_VDD	39	INV_VCC
20	LVDS_VDD	40	NC

3.8.3 Speaker Connector (JSPK1)

Connector Location: JSPK1
Description: Speaker Connector

PIN	ASSIGNMENT
1	VOUTP
2	VOUTN

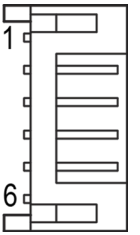


JSPK1

3.8.4 Inverter Connector (JINV1)

Connector Location: JINV1
Description: Inverter Connector

PIN	ASSIGNMENT
1	INV_VCC
2	INV_VCC
3	GND
4	LVDS_BKLCTL
5	GND
6	LVDS_BKLTEN



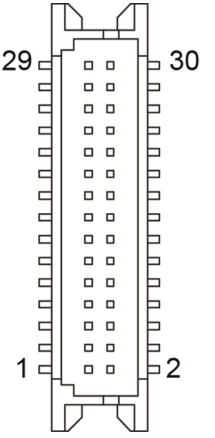
JINV1

3.8.5 LVDS Connector (LVDS1)

Connector Location: LVDS1

Description: LVDS Connector

PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	LVDS_VDD	2	GND
3	LVDS_CLKB_DN	4	LVDS_CLKB_DP
5	GND	6	LVDS_B2_DN
7	LVDS_B2_DP	8	GND
9	LVDS_B1_DN	10	LVDS_B1_DP
11	LVDS_B3_DP	12	LVDS_B3_DN
13	LVDS_B0_DP	14	LVDS_B0_DN
15	GND	16	LVDS_CLKA_DP
17	LVDS_CLKA_DN	18	GND
19	LVDS_A2_DP	20	LVDS_A2_DN
21	GND	22	LVDS_A1_DP
23	LVDS_A1_DN	24	GND
25	LVDS_A0_DP	26	LVDS_A0_DN
27	LVDS_A3_DP	28	LVDS_A3_DN
29	LVDS_VDD	30	LVDS_VDD



LVDS1

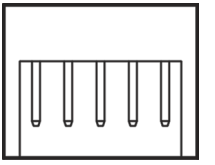
3.8.6 USB 2.0 Connector (JUSB1, JUSB2, JUSB3)

Connector Location: JUSB1, JUSB2, JUSB3

Description: USB 2.0 Connector

JUSB1

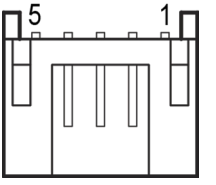
PIN	ASSIGNMENT	PIN	ASSIGNMENT
1	V5P0S_USB2	2	V5P0S_USB1
3	HUB1_DN2	4	HUB1_DN1
5	HUB1_DP2	6	HUB1_DP1
7	GND	8	GND
9	GND	10	GND



JUSB1

JUSB2

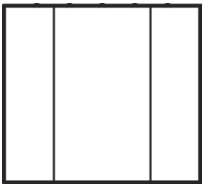
PIN	ASSIGNMENT
1	V5P0S_USB3
2	HUB1_DN3
3	HUB1_DP3
4	GND
5	GND



JUSB2

JUSB3

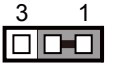
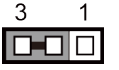
PIN	ASSIGNMENT
1	V5P0S_USB4
2	HUB1_DN42
3	HUB1_DP42
4	GND
5	GND



JUSB3

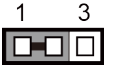
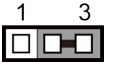
3.8.7 Backlight Voltage Selection (JP_INV1)

Jumper Location: JP_INV1
Description: Backlight Voltage Selection

SELECTION	JUMPER SETTING	JUMPER ILLUSTRATION
5V (VIN_INV)	**1-2** ***(Default Setting)***	 **JP_INV1**
12V (VIN_INV)	2-3	 **JP_INV1**

3.8.8 LVDS Panel Voltage Control Selection (JP_VDD1)

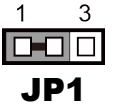
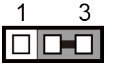
Jumper Location: JP_VDD1
Description: LVDS Panel Voltage Control Selection

SELECTION	JUMPER SETTING	JUMPER ILLUSTRATION
3.3V (LVDS_VDD)	**1-2** ***(Default Setting)***	 **JP_VDD1**
5V (LVDS_VDD)	2-3	 **JP_VDD1**

3.8.9 LVDS Backlight Control Selection (JP1)

Jumper Location: JP1

Description: LVDS Backlight Control Selection

SELECTION	JUMPER SETTING	JUMPER ILLUSTRATION
3.3V (LVDS_BKLCTL)	**1-2** ***(Default Setting)***	 **JP1**
5V (LVDS_BKLCTL)	2-3	 **JP1**

4 Software Utilities

This chapter provides the detailed information that guides users to install driver utilities. The following topics are included:

- Installing Intel® Chipset Software Installation Utility
- Installing Graphics Driver Utility
- Installing Intel® Management Engine Components Driver Installer
- Installing LAN Driver Utility
- Installing Intel® Serial I/O Driver Utility
- Installing Sound Driver Utility

4.1 Introduction

Enclosed with the PA-J501 Series package is our driver utilities, which comes in a DVD-ROM format. Refer to the following table for driver locations

Filename (Assume that DVD- ROM drive is D :)	Purpose
D:\Driver\Platform\1_Main Chip\Win10(64-bit)	Intel(R) Chipset Device Software installer
D:\Driver\Platform\2_Graphics\Win10 (64-bit)	Intel(R) HD Graphics Driver installer
D:\Driver\Platform\3_ME\Win10 (64-bit)\	Intel(R) *Management Engine* Driver installer
D:\Driver\Platform\4_LAN Chip\Win10 (64-bit)	Intel(R) LAN Driver installer
D:\Driver\Platform\5_sound\Win10 (64-bit)	Realtek(R) ALC888S HD Audio Driver installer

4.1.1 Installing Intel® Chipset Software Installation Utility

Introduction

The Intel® Chipset Software Installation Utility installs the Windows *.INF files to the target system. These files outline to the operating system how to configure the Intel chipset components in order to ensure that the following functions work properly:

- SATA Storage Support (SATA & SATA II)
- USB Support (1.1 & 2.0)
- Identification of Intel® Chipset Components in Device Manager

Intel® Chipset Software Installation Utility

The utility pack is to be installed only for Windows 10 64Bit, and it should be installed immediately after the OS installation is finished. Please follow the steps below:

1. Connect the USB DVD-ROM device to PA-J501 and insert the driver disk.
2. Enter the "**Main Chip"** folder where the Chipset driver is located.
3. Click "**SetupChipset.exe"** file for driver installation.
4. Follow the on-screen instructions to install the driver.
5. Once the installation is completed, shut down the system and restart PA-J501 for the changes to take effect.

4.1.2 Installing Graphics Driver Utility

The GRAPHICS interface embedded in PA-J501 can support a wide range of display types. You can have dual displays via LCD and LVDS interfaces and make the system work simultaneously.

To install the Graphics driver utility, follow the steps below:

1. Connect the USB DVD-ROM device to PA-J501 and insert the driver disk.
2. Enter the "**Graphics**" folder where the driver is located
3. Click the "**Installer.exe**" file for Windows 10 platform for driver installation.
4. Follow the on-screen instructions to complete the installation.
5. Once the installation is completed, shut down the system and restart PA-J501 for the changes to take effect.

4.1.3 Intel® Management Engine Components Installer Installation

To install the ME Driver, follow the steps below:

1. Connect the USB DVD-ROM device to PA-J501 and insert the driver disk
2. Enter the "**ME**" folder where the driver is located.
3. Click "**SetupME.exe**" file for driver installation.
4. Follow the on-screen instructions to install the driver.
5. Once the installation is completed, shut down the system and restart PA-J501 for the changes to take effect.

4.1.4 Installing LAN Driver Utility

Follow the steps below to install LAN Driver:

1. Connect the USB DVD-ROM device to PA-J501 and insert the driver disk
2. Enter the "**LAN Chip**" folder where the driver is located.
3. Click "**Wired_driver_27.0_x64.exe**" file for driver installation.
4. Follow the on-screen instructions to install the driver.
5. Once the installation is completed, shut down the system and restart PA-J501 for the changes to take effect.

For more details on the installation procedure, refer to the Readme.txt file that you can fin*d on LAN Driver Utility.*

4.1.5 Installing Sound Driver Utility

The sound function enhanced in this system is fully compatible with Windows 10.

To install the Sound Driver, follow the steps below:

1. Connect the USB DVD-ROM device to PA-J501 and insert the driver disk.
2. Open the "**sound**" folder where the driver is located.
3. Click the "**Setup.exe**" file for driver installation.
4. Follow the on-screen instructions to complete the installation.
5. Once the installation is completed, shut down the system and restart PA-J501 for the changes to take effect.

5 BIOS SETUP

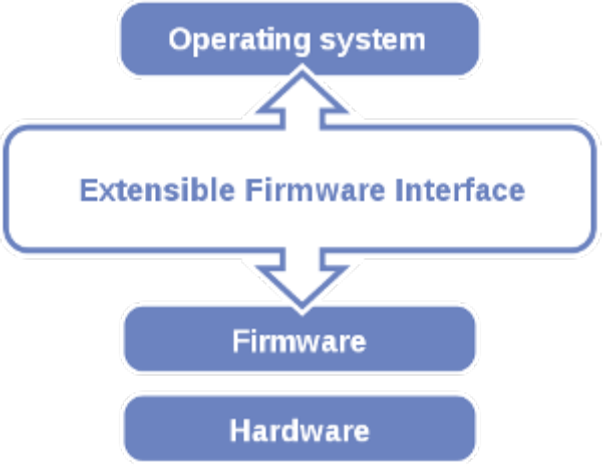
This chapter guides users how to configure the basic system configurations via the BIOS Setup Utilities. The information of the system configuration is saved in BIOS NVRAM so that the Setup information is retained when the system is powered off. The BIOS Setup Utilities consist of the following menu items:

- Main Menu
- Advanced Menu
- Chipset Menu
- Security Menu
- Boot Menu
- Save & Exit Menu

5.1 Introduction

The **PA-J501** uses an AMI Aptio BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated. The SPI Flash contains the BIOS Setup program, Power-on Self-Test (POST), the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support.

Aptio is AMI's BIOS firmware based on the UEFI (Unified Extensible Firmware Interface) Specifications and the Intel Platform Innovation Framework for EFI. The UEFI specification defines an interface between an operating system and platform firmware. The interface consists of data tables that contain platform-related information, boot service calls, and runtime service calls that are available to the operating system and its loader. These elements provide standard environment for booting an operating system and running pre-boot applications. The following diagram shows the Extensible Firmware Interface's location in the software stack.



Extensible Firmware Interface Diagram

EFI BIOS provides an user interface allow users the ability to modify hardware configuration, e.g. change the system date and time, enable or disable a system component, decide bootable device priorities, setup personal password, etc., which is convenient for modifications and customization of the computer system and allows technicians another method for finding solutions if hardware has any problems.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <Del> or <ESC> key after the POST memory test begins and before the operating system boot begins. The settings are shown below.

Users will need to set up the system configuration from the BIOS Setup Utility when any of the following conditions occurs:

1. You are starting your system for the first time.
2. You have changed the hardware in your system or the hardware becomes faulty.
3. The system configuration is reset after the user configures to clear CMOS data via the JCMOS1 jumper.
4. The power of the CMOS RAM became lost and the system configuration has been erased.

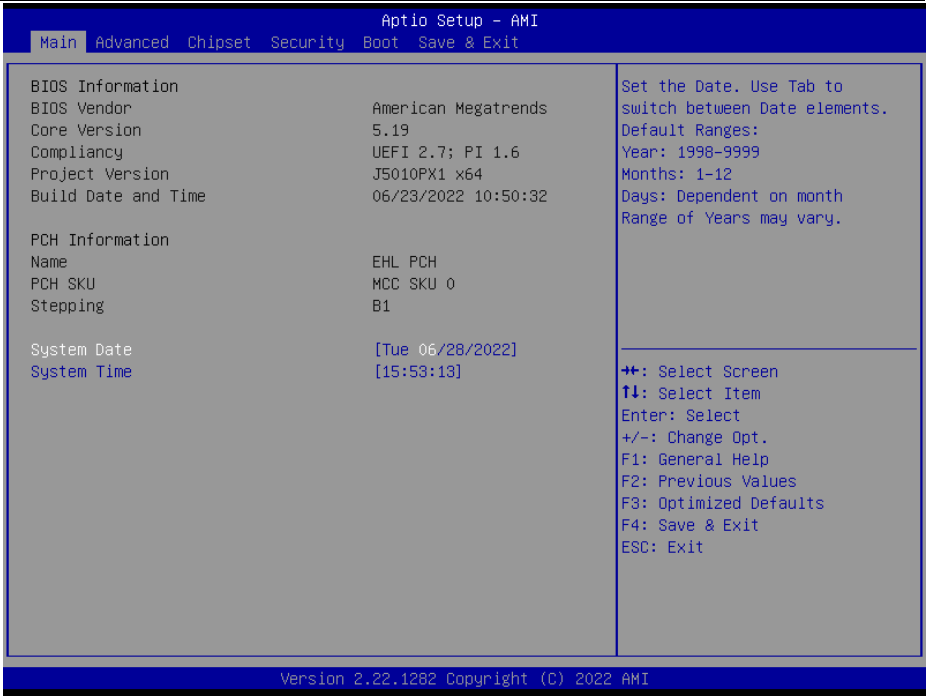
All the menu settings are described in details in this chapter.

5.1.1.1 Accessing Setup Utility

When the system is powered on, the BIOS will enter the Power-On Self Test (POST) routines and the following message will appear on the lower screen:

POST Screen with AMI Logo

As long as this message is present on the screen you may press the <Del> key (the one that shares the decimal point at the bottom of the number keypad) to access the Setup program. In a moment, the main menu of the Aptio Setup Utility will appear on the screen:



BIOS Setup Menu Initialization Screen

You may move the cursor by up/down keys to highlight the individual menu items. As you highlight each item, a brief description of the highlighted selection will appear at the bottom of the screen.

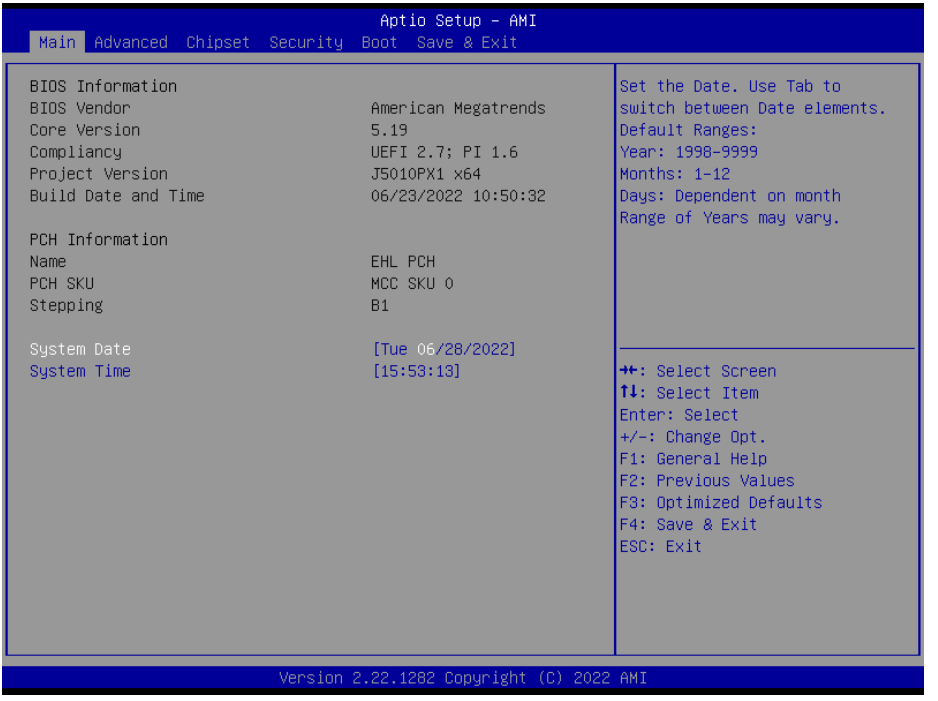
The language of the BIOS setup menu interface and help messages are shown in US English. You may use <↑> or <↓> key to select among the items and press <Enter> to confirm and enter the sub-menu. The following table provides the list of the navigation keys that you can use while operating the BIOS setup menu.

BIOS Setup Navigation Key	Description
<←> and <→>	Select a different menu screen (move the cursor from the selected menu to the left or right).
<↑> and <↓>	Select a different item (move the cursor from the selected item upwards or downwards)
<Enter>	Execute the command or select the sub-menu.
<F2>	Load the previous configuration values.
<F3>	Load the default configuration values.
<F4>	Save the current values and exit the BIOS setup menu.
<Esc>	Close the sub-menu. Trigger the confirmation to exit BIOS setup menu.

5.1.2 Main

Menu Path *Main*

The **Main** menu allows you to view the BIOS Information and change the system date and time. Use tab to switch between date elements. Use <↑> or <↓> arrow keys to highlight the item and enter the value you want in each item. This screen also displays the BIOS version (project) and BIOS Build Date and Time.



BIOS Main Menu

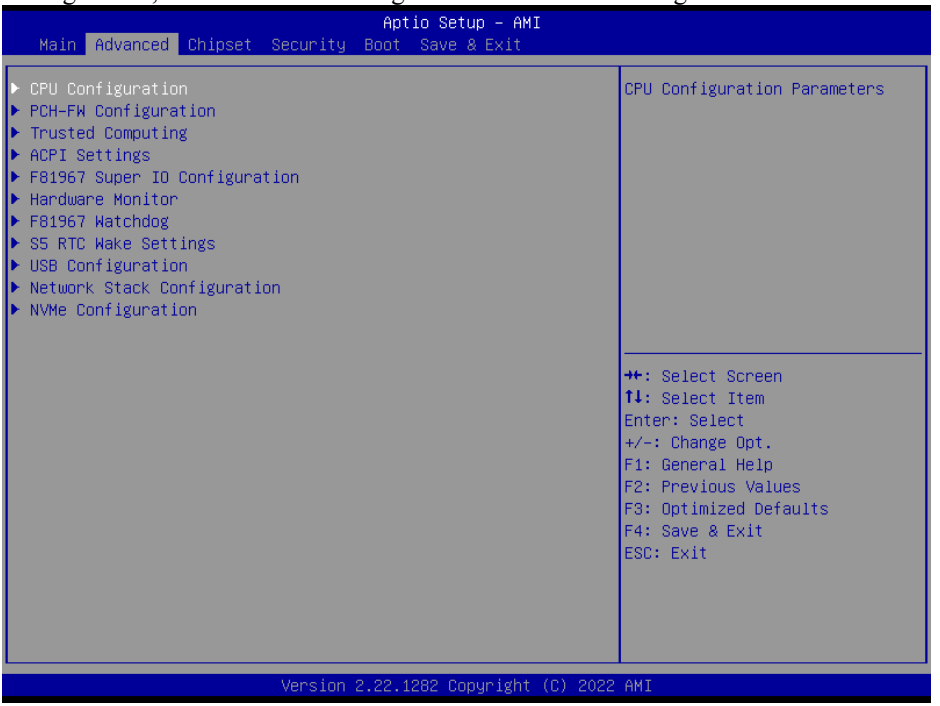
BIOS Setting	Options	Description/Purpose
BIOS Vendor	No changeable options	Displays the BIOS vendor.
Core Version	No changeable options	Displays the current BIOS core version.
Compliancy	No changeable options	Displays the current UEFI version.
Project Version	No changeable options	Displays the version of the BIOS currently installed on the platform.
Build Date and Time	No changeable options	Displays the date of the current BIOS version.
Name	No changeable options	Displays the name of the PCH
PCH SKU	No changeable options	Displays the SKU for the PCH

BIOS Setting	Options	Description/Purpose
Stepping	No changeable options	Displays the stepping of the PCH
System Date	month, day, year	Sets the current date. The format is [Day Month/Date/ Year]. Users can directly enter values or use <+> or <-> arrow keys to increase/decrease it. The "Day" is automatically changed.
System Time	hour, minute, second	Sets the clock of the system. The format is [Hour: Minute: Second]. Users can directly enter values or use <+> or <-> arrow keys to increase/decrease it.

5.1.3 Advanced

Menu Path *Advanced*

This menu provides advanced the sub-menu items such as CPU Configuration, PCH-FW Configuration, Trusted Computing, ACPI Settings, F81967 Super IO Configuration, Hardware Monitor, F81967 Watchdog, S5 RTC Wake Settings, USB Configuration, Network Stack Configuration and NVMe Configuration.



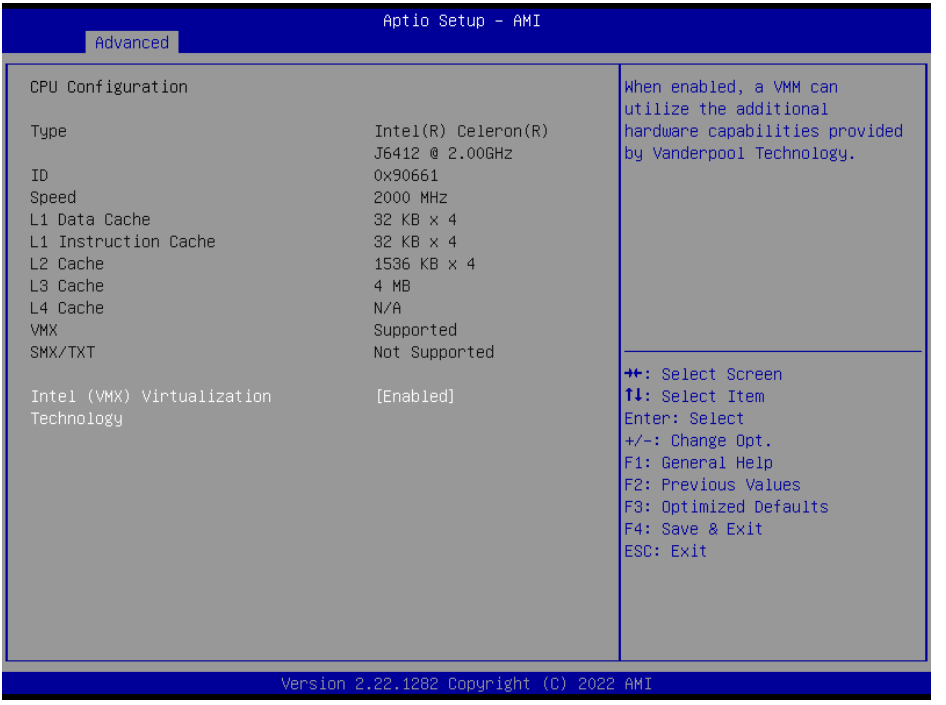
BIOS Advanced Menu

BIOS Setting	Options	Description/Purpose
CPU Configuration	Sub-Menu	CPU Configuration Parameters.
PCH-FW Configuration	Sub-Menu	Management Engine Technology Parameters.
Trusted Computing	Sub-Menu	Trusted Computing Settings.
ACPI Settings	Sub-Menu	System ACPI Parameters.
F81967 Super IO Configuration	Sub-Menu	System Super IO Chip parameters.
Hardware Monitor	Sub-Menu	Monitor hardware status.
F81967 Watchdog	Sub-Menu	F81967 Watchdog parameters.
S5 RTC Wake Settings	Sub-Menu	S5 RTC Wake Parameters.
USB Configuration	Sub-Menu	USB Configuration Parameters.
Network Stack Configuration	Sub-Menu	Network Stack Settings.
NVMe Configuration	Sub-Menu	NVMe Device Options Settings.

5.1.3.1 Advanced - CPU Configuration

Menu Path *Advanced > CPU Configuration*

The **CPU Configuration** provides advanced CPU settings and some information about CPU.



CPU Configuration Screen

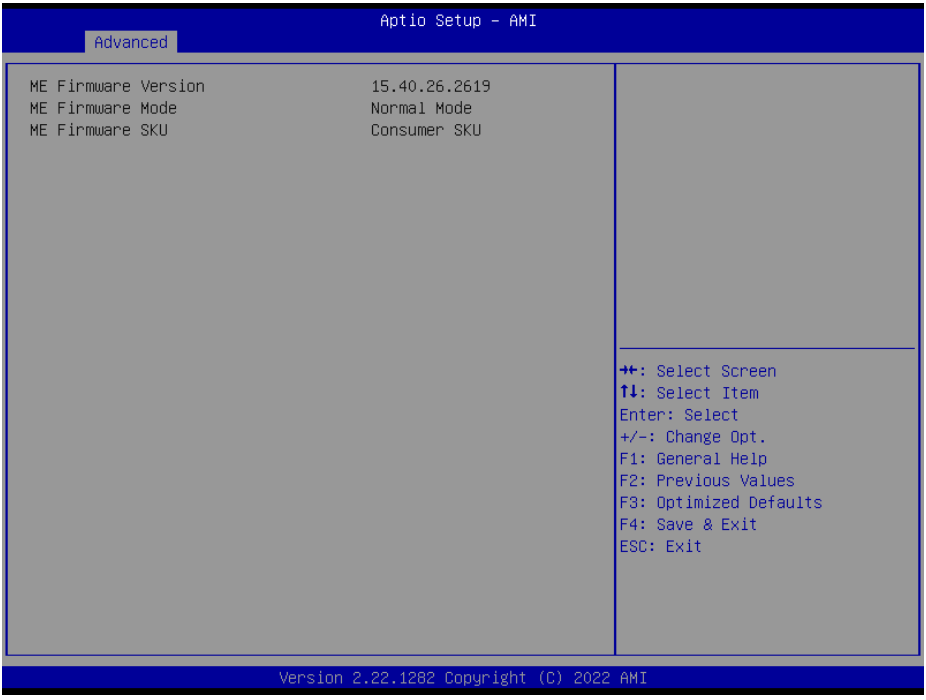
BIOS Setting	Options	Description/Purpose
Type	No changeable options	Displays the CPU Type.
ID	No changeable options	Displays the CPU ID.
Speed	No changeable options	Displays the CPU Speed.
L1 Data Cache	No changeable options	Displays the size of L1 Data Cache
L1 Instruction Cache	No changeable options	Displays the size of L1 Instruction Cache
L2 Cache	No changeable options	Displays the size of L2 Cache.
L3 Cache	No changeable options	Displays the size of L3 Cache.
L4 Cache	No changeable options	Displays the size of L4 Cache.
VMX	No changeable options	CPU/VMX hardware support for virtual machines.
SMX/TXT	No changeable options	Secure Mode extensions support.

BIOS Setting	Options	Description/Purpose
Intel (VMX) Virtualization Technology	- Disabled - Enabled (default)	When enabled, VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

5.1.3.2 Advanced - PCH-FW Configuration

Menu Path *Advanced > PCH-FW Configuration*

The **PCH-FW** allows users to view the information about ME (Management Engine) firmware information, such ME firmware version, firmware mode and firmware SKU.



PCH-FW Configuration Screen

BIOS Setting	Options	Description/Purpose
ME Firmware Version	No changeable options	Displays the ME Firmware Version.
ME Firmware Mode	No changeable options	Displays the ME Firmware Mode.
ME Firmware SKU	No changeable options	Displays the ME Firmware SKU.

5.1.3.3 Advanced - Trusted Computing

Menu Path *Advanced > Trusted Computing*

The **Trusted Computing** allows users to enable / disable BIOS support for security device. The operating system will now show Security Device. The TCG EFI protocol and INT1A interface will not be available.

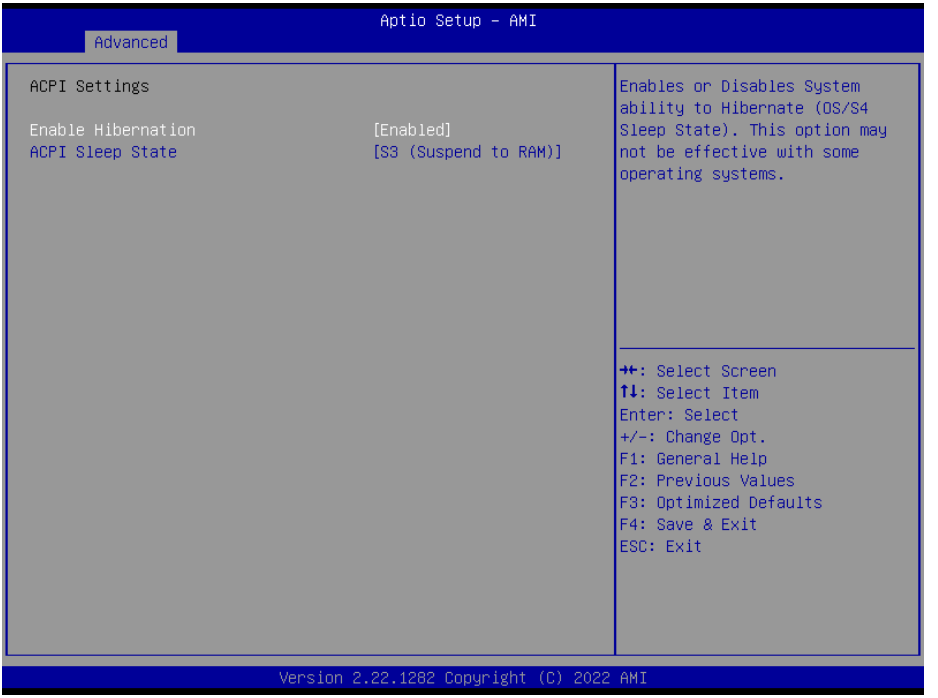
Trusted Computing Screen

BIOS Setting	Options	Description/Purpose
Firmware Version	No changeable options	Displays the Firmware Version.
Vendor	No changeable options	Displays the Vendor.
Security Device Support	- Disabled - Enable (Default)	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
Active PCR banks	No changeable options	Displays the Active PCR banks.
Available PCR banks	No changeable options	Displays the Available PCR banks.
SHA256 PCR Bank	- Disabled - Enabled (Default)	Enables or Disables SHA256 PCR Bank.

5.1.3.4 Advanced - ACPI Settings

Menu Path *Advanced > ACPI Settings*

The **ACPI Settings** allows users to configure relevant ACPI (Advanced Configuration and Power Management Interface) settings, such as enable / disable Hibernation and ACPI Sleep State.



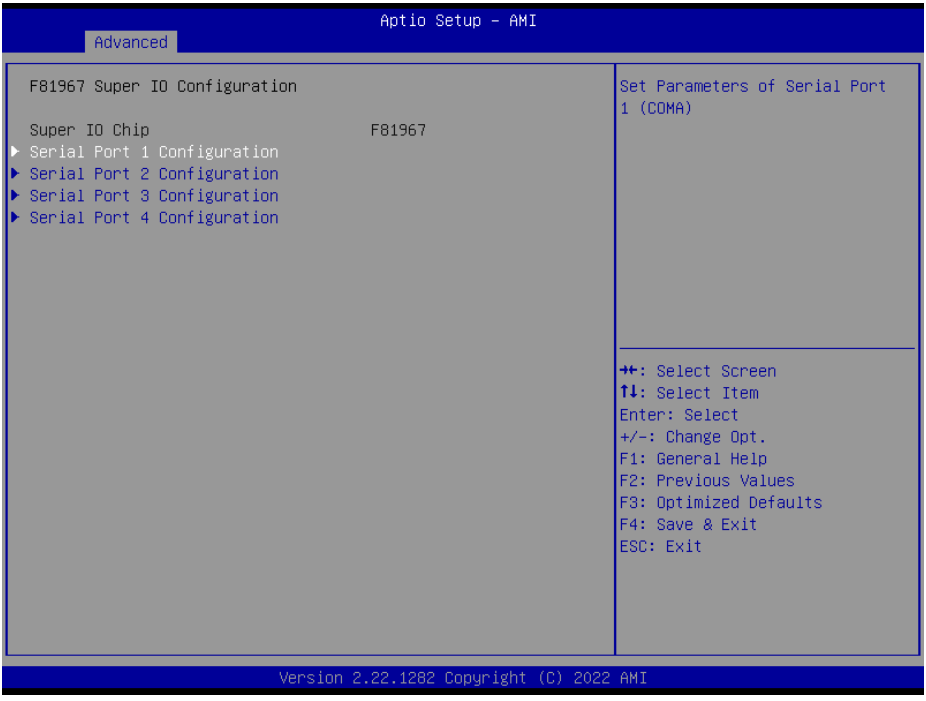
ACPI Settings Screen

BIOS Setting	Options	Description/Purpose
Enable Hibernation	- Disabled - Enabled (Default)	Enables or disables the system's ability to hibernate (OS / S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	- Suspend Disabled - S3 (Suspend to RAM) (Default)	Selects the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

5.1.3.5 Advanced - F81967 Super IO Configuration

Menu Path *Advanced > F81967 Super IO Configuration*

The **F81967 Super IO Configuration** allows users to configure the serial ports 1-4.

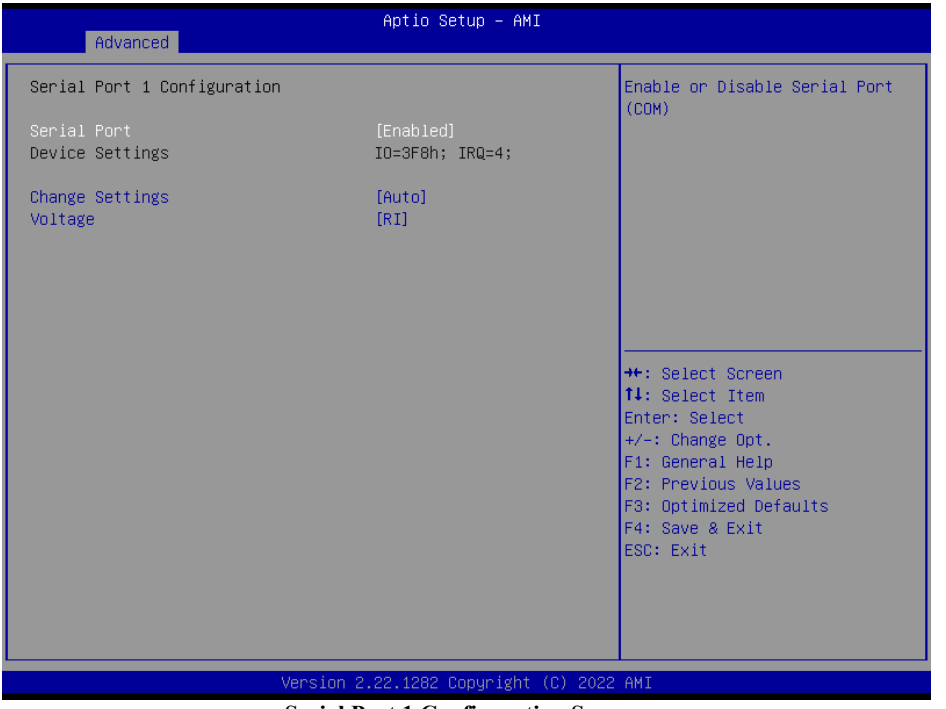


F81967 Super IO Configuration Screen

BIOS Setting	Options	Description/Purpose
Serial Port 1 Configuration	Sub-Menu	Configure the parameters of Serial Port 1 (COM1).
Serial Port 2 Configuration	Sub-Menu	Configure the parameters of Serial Port 2 (COM2).
Serial Port 3 Configuration	Sub-Menu	Configure the parameters of Serial Port 3 (COM3).
Serial Port 4 Configuration	Sub-Menu	Configure the parameters of Serial Port 4 (COM4).

F81967 Super IO Configuration – Serial Port 1 Configuration

Menu Path *Advanced > F81967 Super IO Configuration > Serial Port 1 Configuration*

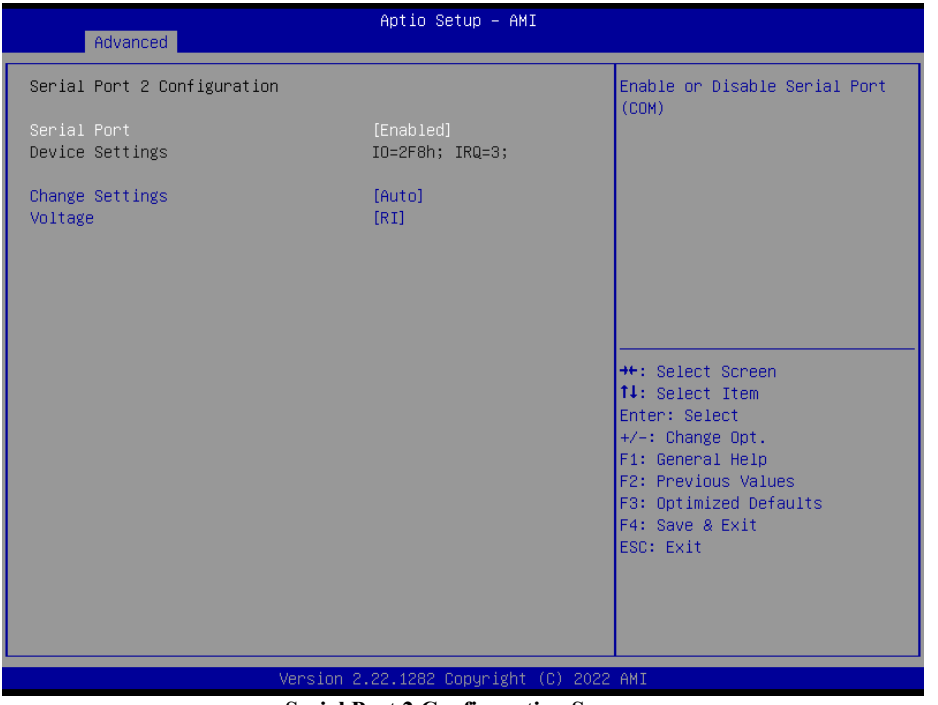


Serial Port 1 Configuration Screen

BIOS Setting	Options	Description/Purpose
Serial Port	- Disabled - Enabled (Default)	Enables or disables Serial Port 1.
Device Settings	No changeable options	Displays the current settings of Serial Port 1.
Change Settings	- Auto (Default) - IO=3F8h; IRQ=4; - IO=3F8h; IRQ=3,4,5,6,7,9,10,11.12; - IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12; - IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12; - IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;	Selects IRQ and I/O resource settings for Serial Port 1.
Voltage	- RI (Default) - 5V - 12V	Selects COM port voltage

F81967 Super IO Configuration – Serial Port 2 Configuration

Menu Path *Advanced > F81967 Super IO Configuration > Serial Port 2 Configuration*

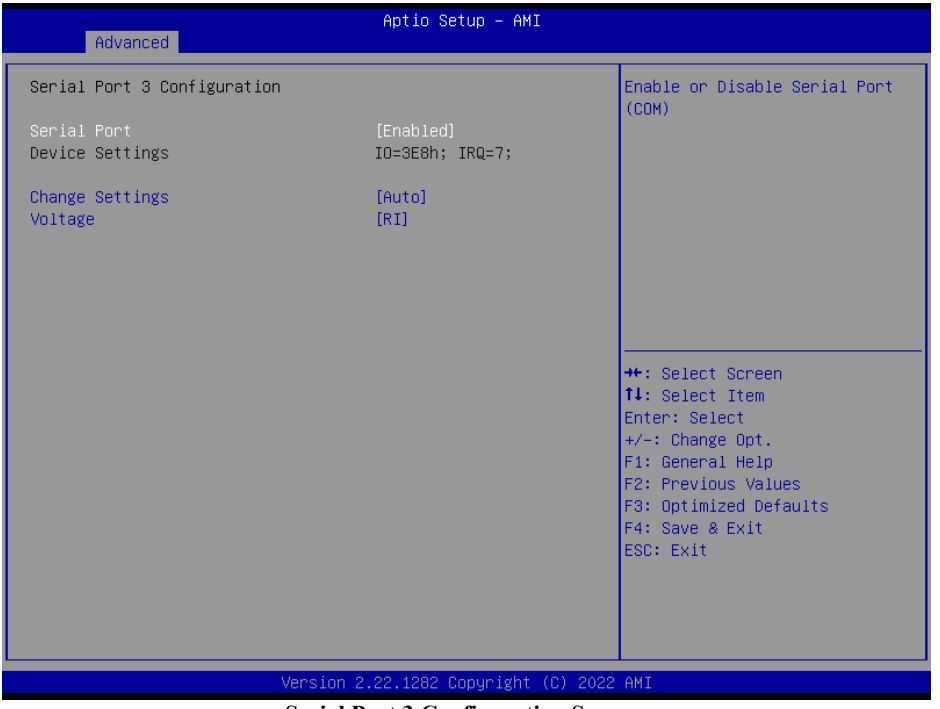


Serial Port 2 Configuration Screen

BIOS Setting	Options	Description/Purpose
Serial Port	- Disabled - Enabled (Default)	Enables or disables Serial Port 2.
Device Settings	No changeable options	Displays the current settings of Serial Port 2.
Change Settings	- Auto (Default) - IO=2F8h; IRQ=3; - IO=3F8h; IRQ=3,4,5,6,7,9,10,11.12; - IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12; - IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12; - IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;	Selects IRQ and I/O resource for the serial port 2.
Voltage	- RI (Default) - 5V - 12V	Selects COM port voltage

F81967 Super IO Configuration – Serial Port 3 Configuration

Menu Path *Advanced > F81967 Super IO Configuration > Serial Port 3 Configuration*

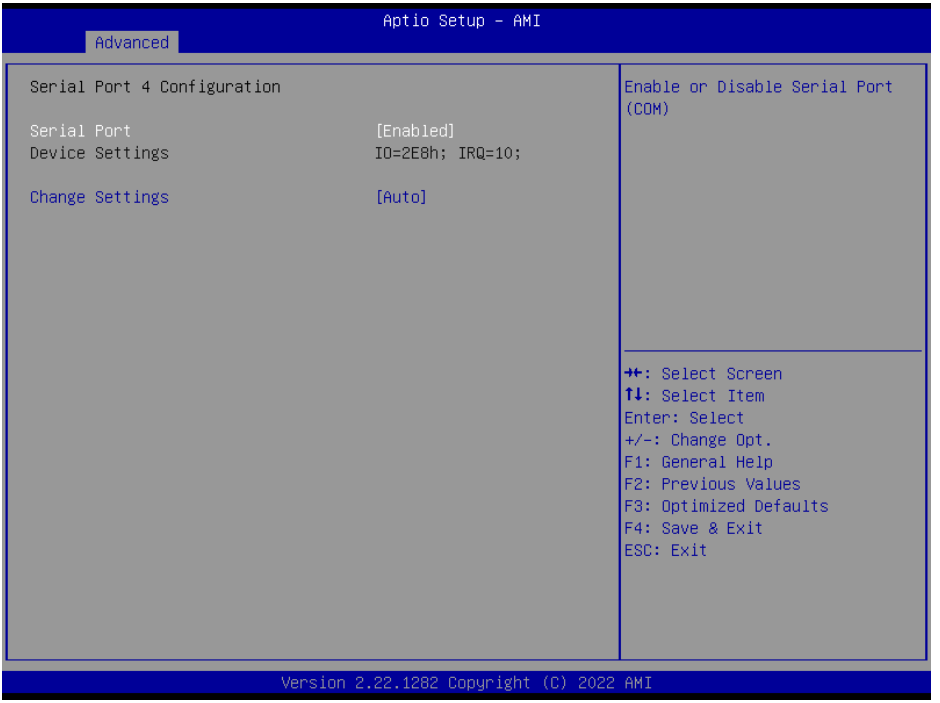


Serial Port 3 Configuration Screen

BIOS Setting	Options	Description/Purpose
Serial Port	- Disabled - Enabled (Default)	Enables or disables Serial Port 3.
Device Settings	No changeable options	Displays the current settings of Serial Port 3.
Change Settings	- Auto (Default) - IO=3E8h; IRQ=7; - IO=3E8h; IRQ=3,4,5,6,7,9,10,11.12; - IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; - IO=3F0h; IRQ=3,4,5,6,7,9,10,11,12; - IO=2E0h; IRQ=3,4,5,6,7,9,10,11,12;	Selects IRQ and I/O resource for the serial port 3.
Voltage	- RI (Default) - 5V - 12V	Selects COM port voltage

F81967 Super IO Configuration – Serial Port 4 Configuration

Menu Path *Advanced > F81967 Super IO Configuration > Serial Port 4 Configuration*



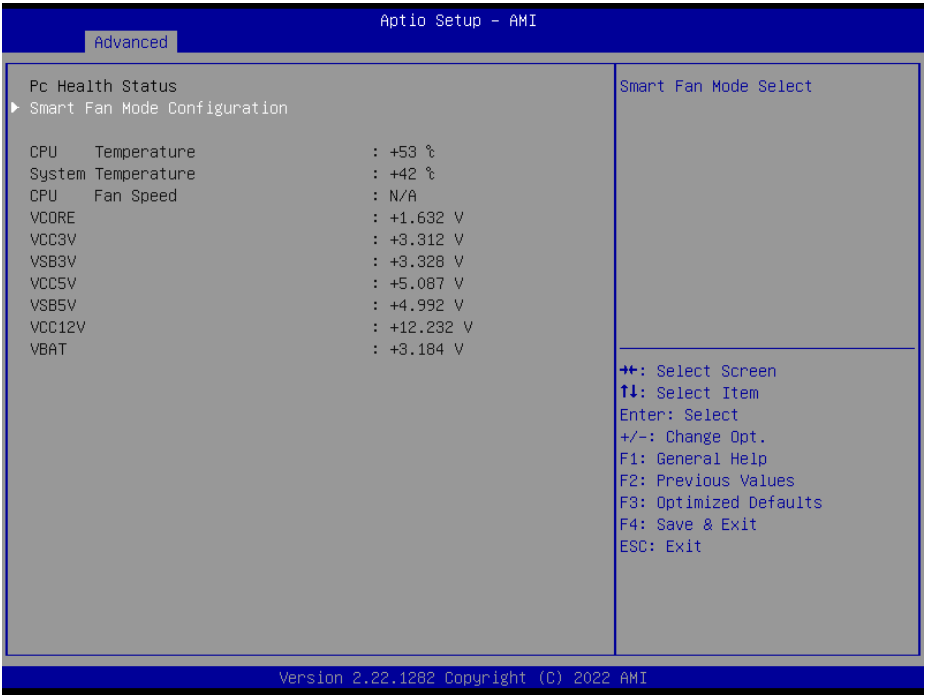
Serial Port 4 Configuration Screen

BIOS Setting	Options	Description/Purpose
Serial Port	- Disabled - Enabled (Default)	Enables or disables Serial Port 4.
Device Settings	No changeable options	Displays the current settings of Serial Port 4.
Change Settings	- Auto (Default) - IO=2E8h; IRQ=7; - IO=3E8h; IRQ=3,4,5,6,7,9,10,11.12; - IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12; - IO=2F0h; IRQ=3,4,5,6,7,9,10,11,12; - IO=2E0h; IRQ=3,4,5,6,7,9,10,11,12;	Selects IRQ and I/O resource for the serial port 4.

5.1.3.6 Advanced - Hardware Monitor

Menu Path *Advanced > Hardware Monitor*

The **Hardware Monitor** allows users to monitor the health and status of the system such as CPU temperature, system temperature, CPU fan speed, and voltage levels in supply.



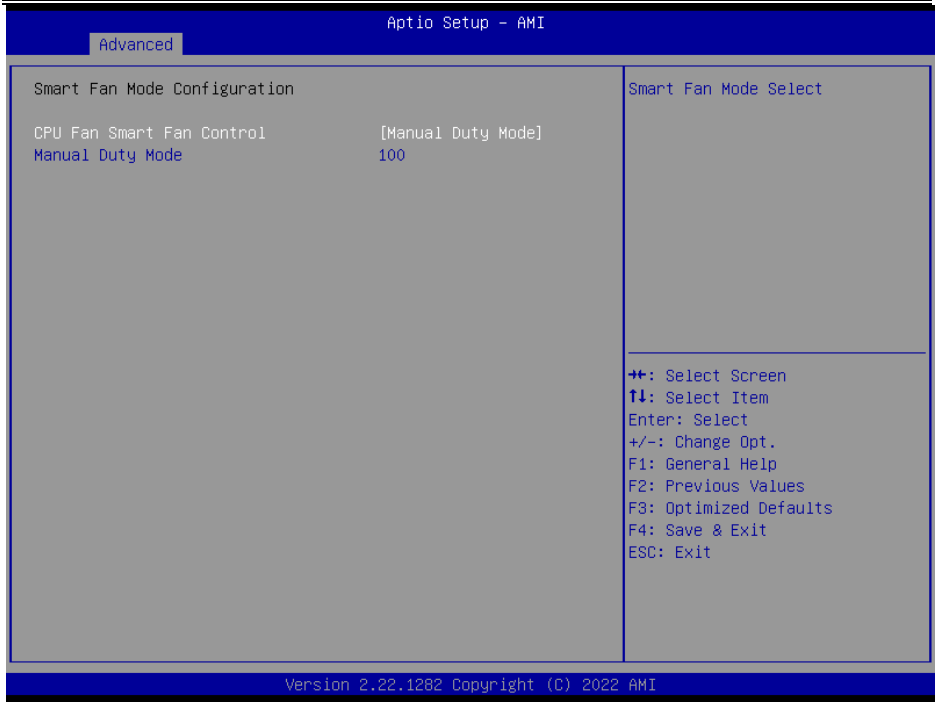
Hardware Monitor Screen

BIOS Setting	Options	Description/Purpose
Smart Fan Mode Configuration	Sub-Menu	Smart Fan Mode Selection. **Note:** No CPU Fan is used on PA-J501.
CPU Temperature	No changeable options	Displays the processor's temperature.
System Temperature	No changeable options	Displays the system's temperature.
CPU Fan Speed	No changeable options	Displays CPU Fan speed. **Note:** Because no CPU Fan is used on PA-J501, so "**N/A**" is shown for this item.
VCORE	No changeable options	Detects and displays the voltage level of VCORE in supply.

BIOS Setting	Options	Description/Purpose
VCC3V	No changeable options	Detects and displays the voltage level of VCC3V in supply.
VSB3V	No changeable options	Detects and displays the voltage level of VSB3V in supply.
VCC5V	No changeable options	Detects and displays the voltage level of VCC5V in supply.
VSB5V	No changeable options	Detects and displays the voltage level of VSB5V in supply.
VCC12V	No changeable options	Detects and displays the voltage level of VCC12 in supply.
VBAT	No changeable options	Detects and displays the voltage level of VBAT in supply.

Smart Fan Mode Configuration

Menu Path *Advanced > Hardware Monitor > Smart Fan Mode Configuration*



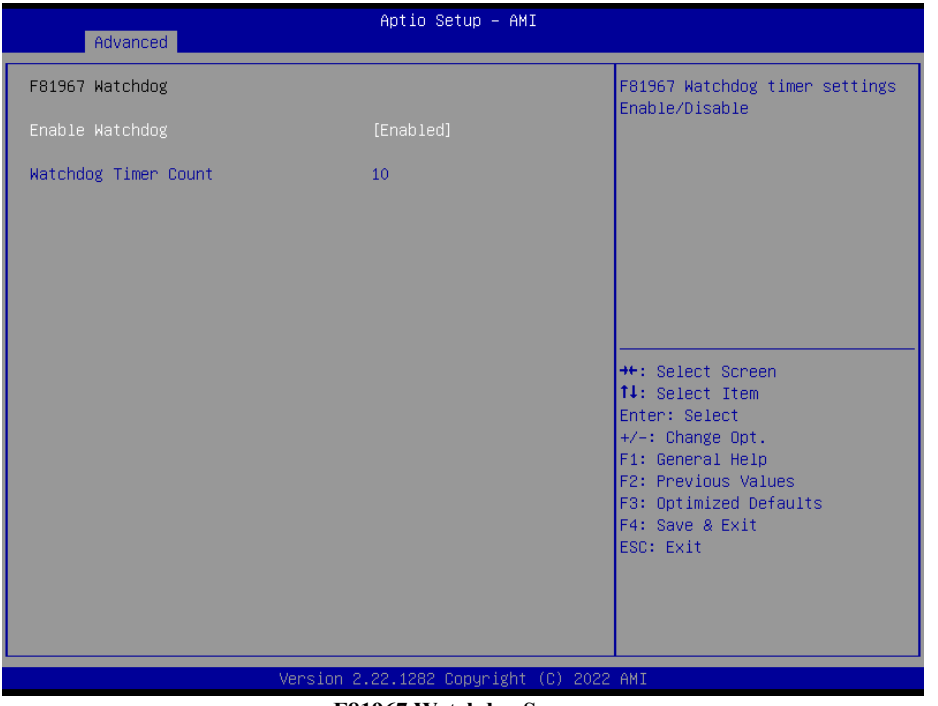
Smart Fan Mode Configuration Screen

BIOS Setting	Options	Description/Purpose
CPU Fan Smart Fan Control	- Manual Duty Mode - Auto Duty-Cycle Mode (Default)	Smart Fan Mode select for CPU Fan.
Manual Duty Mode	Numeric (from 1 to 100)	Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100.
Temperature 1~4	Numeric (from 1 to 100)	Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100.
Duty Cycle 1~4	Numeric (from 1 to 100)	Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100.

5.1.3.7 Advanced - F81967 Watchdog

Menu Path *Advanced > F81967 Watchdog*

If the system hangs or fails to respond, enable the F81967 watchdog function to trigger a system reset via the 255-level watchdog timer.

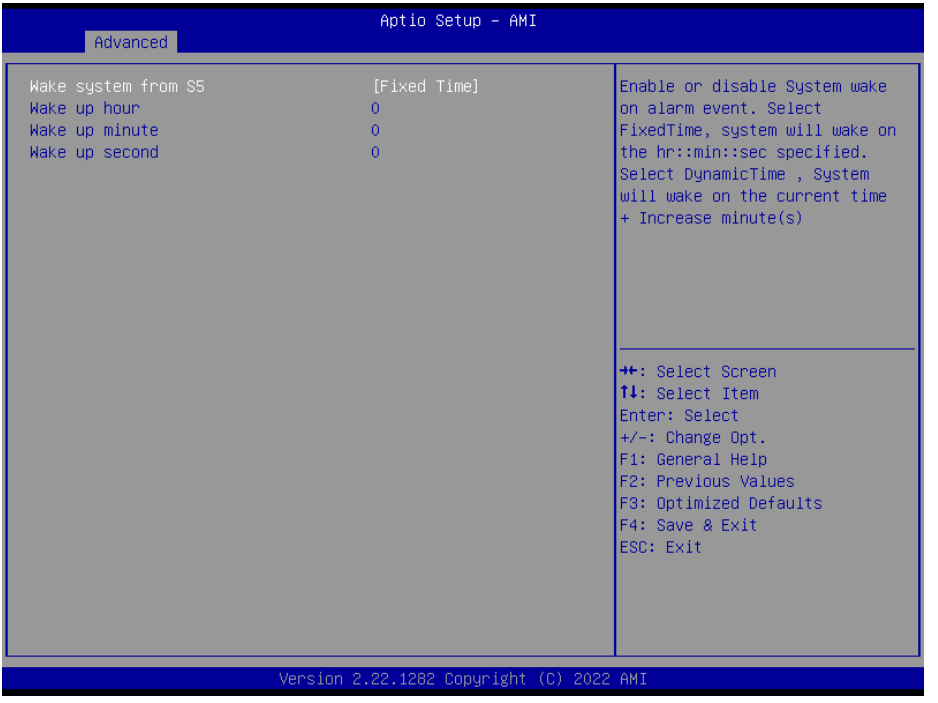


F81967 Watchdog Screen

BIOS Setting	Options	Description/Purpose
Enable Watchdog	- Enabled - Disabled (Default)	Enables / Disables F81967 Watchdog timer.
Watchdog Timer Count	Numeric (from 10 to 255)	The number of count for Timer.

5.1.3.8 Advanced - S5 RTC Wake Settings

Menu Path *Advanced > S5 RTC Wake Settings*



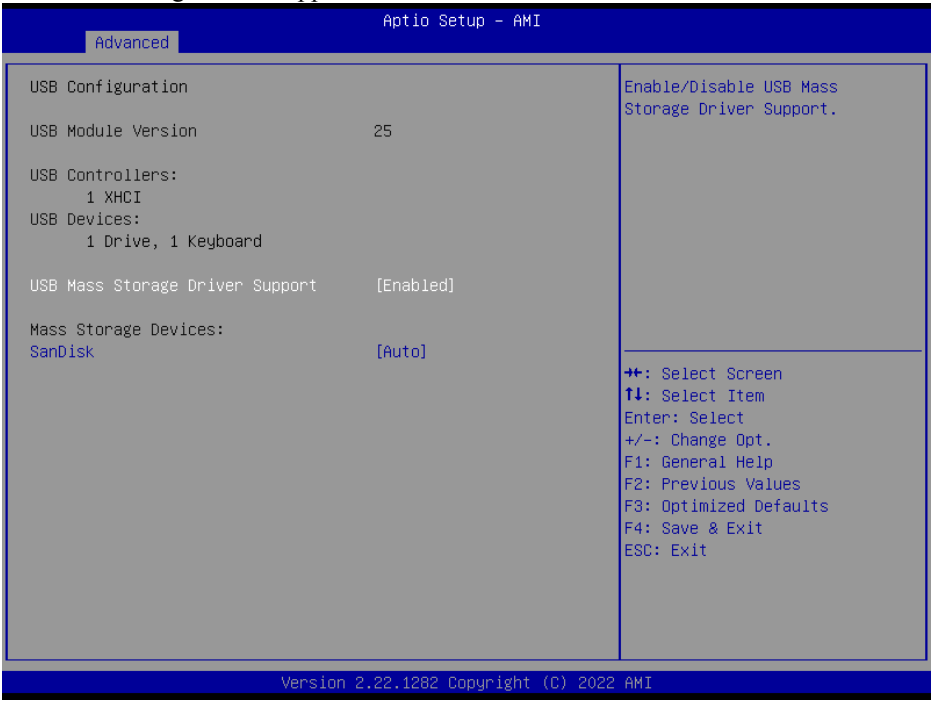
S5 RTC Wake Settings Screen

BIOS Setting	Options	Description/Purpose
Wake system from S5	- Disabled (default) - Fixed Time - Dynamic Time	Enables or disables System wake on alarm event. • **Fixed Time:** The system will wake on the time (hr::min::sec) specified. • **Dynamic Time:** The system will wake on the current time + Increase minute(s).
Wake up hour	Numeric (from 0 to 23)	Enters **0-23** to set the wake-up hour, e.g.: enters 3 for 3 a.m. and 15 for 3 pm
Wake up minute	Numeric (from 0 to 59)	Enters **0-59** to set the wake-up minute.
Wake up second	Numeric (from 0 to 59)	Enters **0-59** to set the wake-up second.
Wake up minute increase	Numeric (from 1 to 5)	Enters **1-5** to set the increased minute(s) for dynamic wake-up time.

5.1.3.9 Advanced - USB Configuration

Menu Path *Advanced > USB Configuration*

The **USB Configuration** allows users to configure advanced USB settings such as USB mass storage driver support.

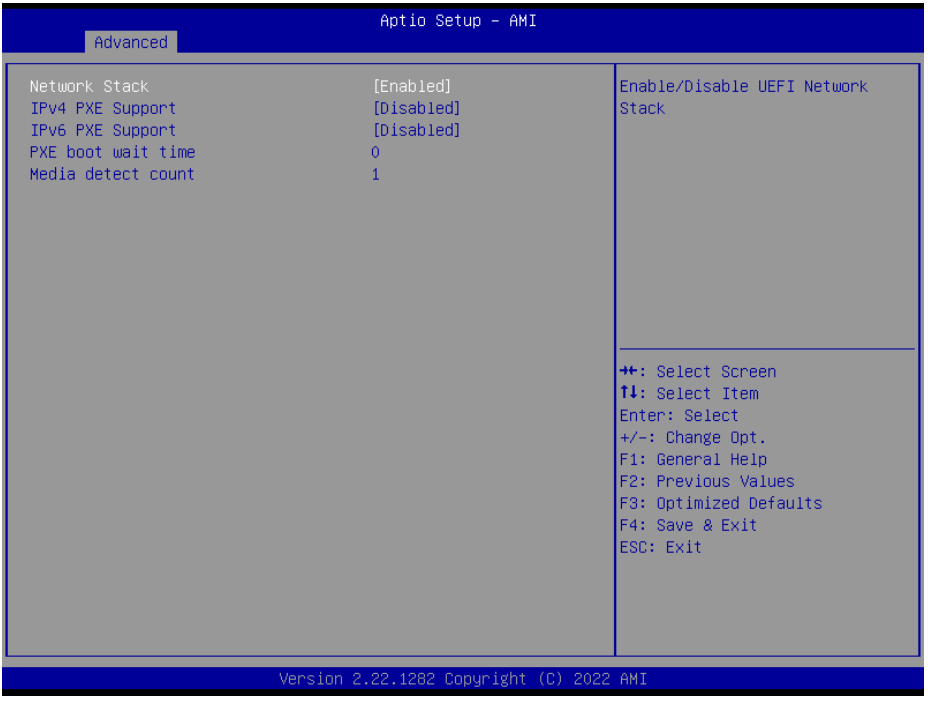


USB Configuration Screen

BIOS Setting	Options	Description/Purpose
USB Module Version	No changeable options	Displays USB module version.
USB Controllers	No changeable options	Displays number and type of USB controllers (if any).
USB Devices	No changeable options	Displays number and type of connected USB devices (if any).
USB Mass Storage Driver Support	- Disabled - Enabled (Default)	Enables / Disables USB Mass Storage Driver Support.
Mass Storage Devices: [drive(s)]	- Auto (Default) - Floppy - Forced FDD - Hard Disk - CD-ROM	**'AUTO'** enumerates devices according to their media format. Optical drives are emulated as **'CD-ROM'**. Drives with no media will be emulated according to a drive type.

5.1.3.10 Advanced - Network Stack Configuration

Menu Path *Advanced > Network Stack Configuration*



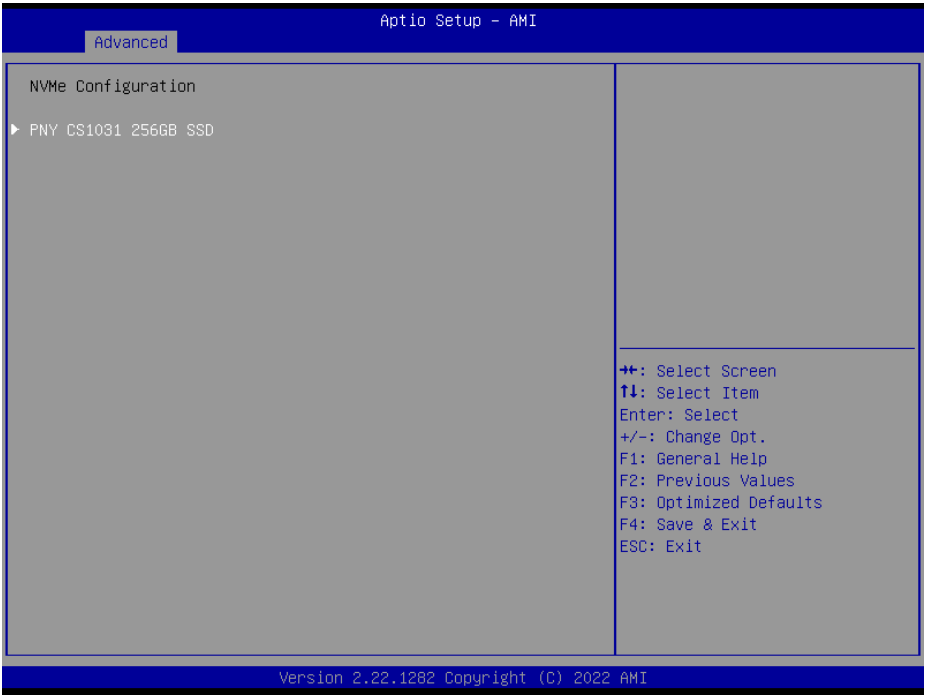
Network Stack Configuration Screen

BIOS Setting	Options	Description/Purpose
Network Stack	- Disabled (Default) - Enabled	Enables or Disables UEFI Network Stack.
Ipv4 PXE Support	- Disabled (Default) - Enabled	Enables Ipv4 PXE Boot Support. If disabled, Ipv4 PXE boot option will not be created.
Ipv6 PXE Support	- Disabled (Default) - Enabled	Enables Ipv6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created.
PXE boot wait time	Numeric (from 0 to 5)	Wait time to press ESC key to abort the PXE boot.
Media detect count	Numeric (from 1 to 50)	Numbers of times presence of media will be checked.

5.1.3.11 Advanced - NVMe Configuration

Menu Path *Advanced > NVMe Configuration*

The **NVMe Configuration** allows users to view the information about NVMe Device.



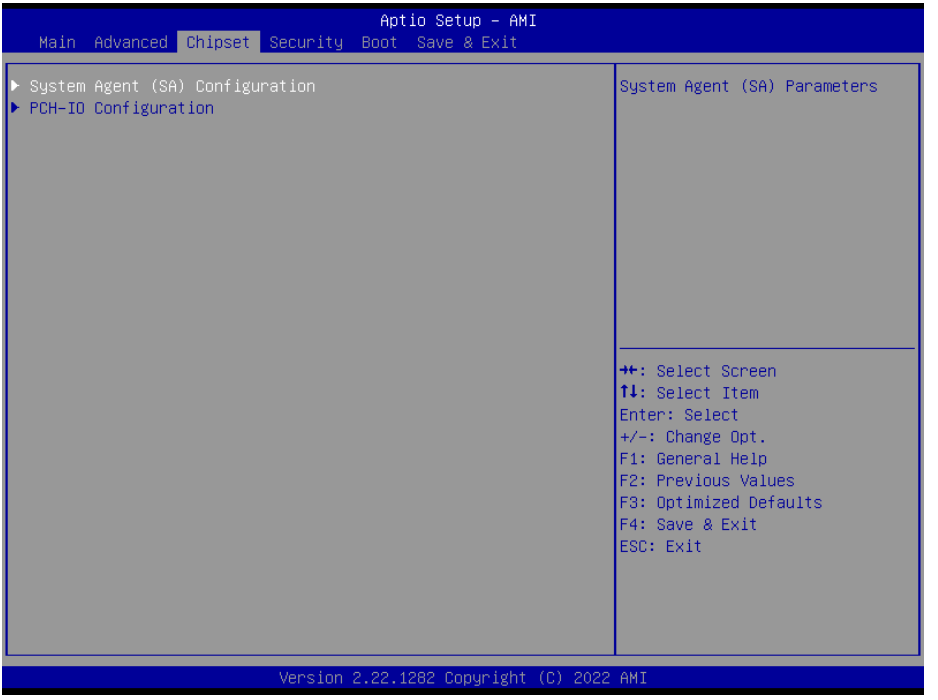
NVMe Configuration Screen

BIOS Setting	Options	Description/Purpose
NVMe Configuration	No changeable options	Displays NVMe device.

5.1.4 Chipset

Menu Path *Chipset*

This menu allows users to configure advanced Chipset settings such as System Agent (SA) and PCH-IO configuration parameters.



Chipset Menu Screen

BIOS Setting	Options	Description/Purpose
System Agent (SA) Parameters	Sub-Menu	Sets the Parameter for System Agent (SA) configuration.
PCH-IO Configuration	Sub-Menu	Sets the Parameter for PCH configuration.

5.1.4.1 System Agent (SA) Configuration

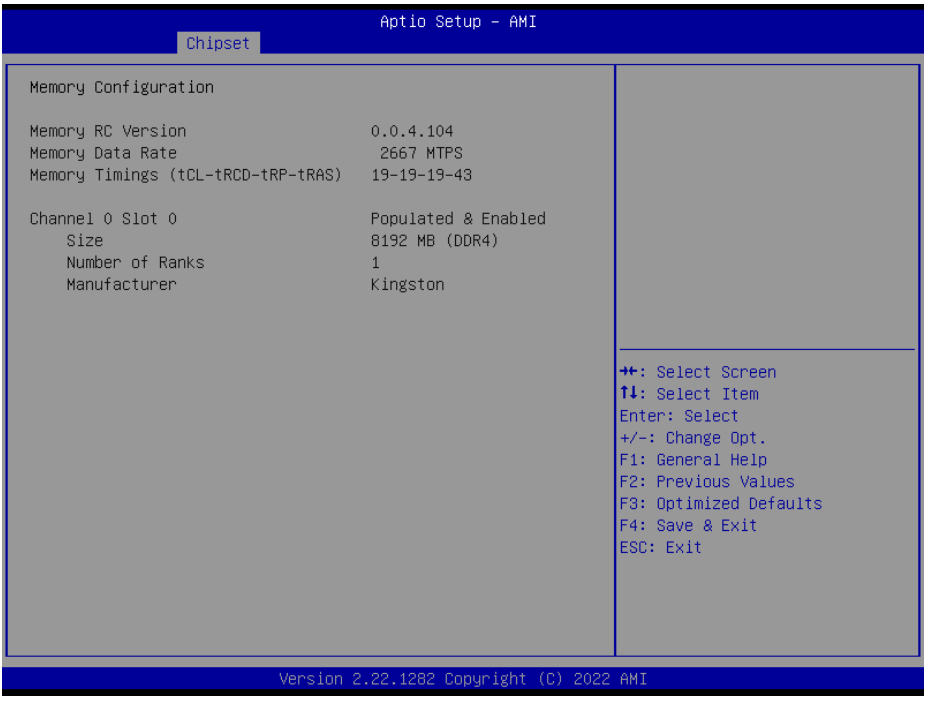
Menu Path *Chipset > System Agent (SA) Configuration*

System Agent (SA) Configuration Screen

BIOS Setting	Options	Description/Purpose
Memory Configuration	Sub-Menu	Memory Configuration parameters
VT-d	- Disabled - Enabled (Default)	Enables or Disables VT-d function.

System Agent (SA) Configuration – Memory Configuration

Menu Path *Chipset > System Agent (SA) Configuration > Memory Configuration*



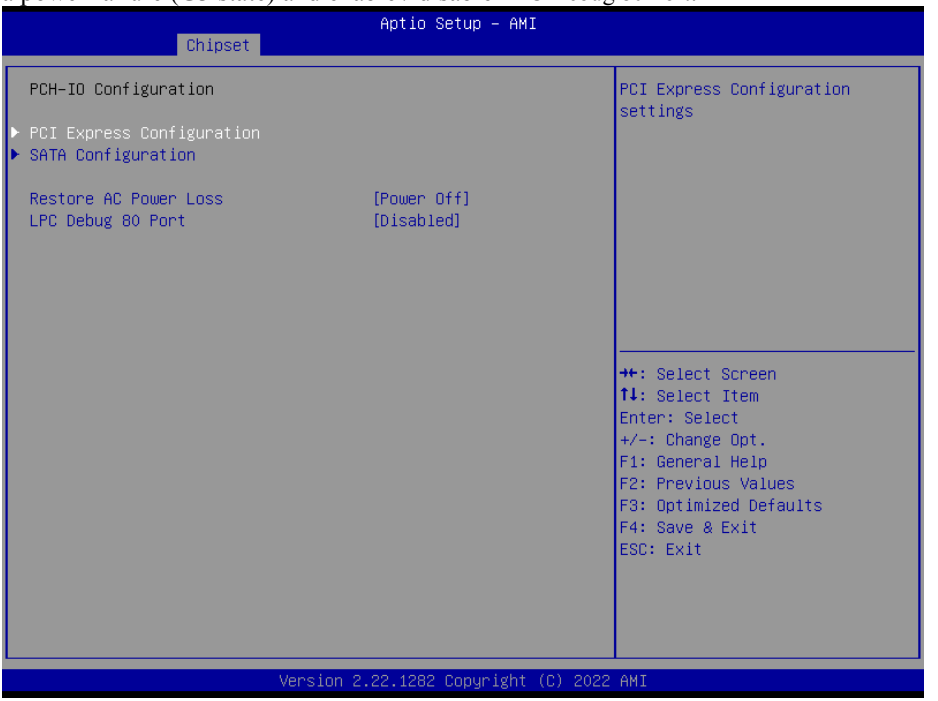
Memory Configuration Screen

BIOS Setting	Options	Description/Purpose
Memory RC Version	No changeable options	Displays the Memory RC Version.
Memory Data Rate	No changeable options	Displays the Frequency of Memory.
Memory Timing (tCL-tRCD-tRP-tRAS)	No changeable options	Displays the Timings of Memory.
Channel 0 Slot 0	No changeable options	Displays the Channel Slot Subtitle.
Size	No changeable options	Displays the Memory size in the slot.
Number of Ranks	No changeable options	Displays the Number of Ranks in the slot.
Manufacturer	No changeable options	Display the DIMM Manufacturer name.

5.1.4.2 PCH IO Configuration

Menu Path *Chipset > PCH IO Configuration*

The **PCH-IO Configuration** allows users to configure PCI Express configuration, SATA settings, determine the power on/off state that the system will go to following a power failure (G3 state) and enable / disable LPC Debug 80 Port.

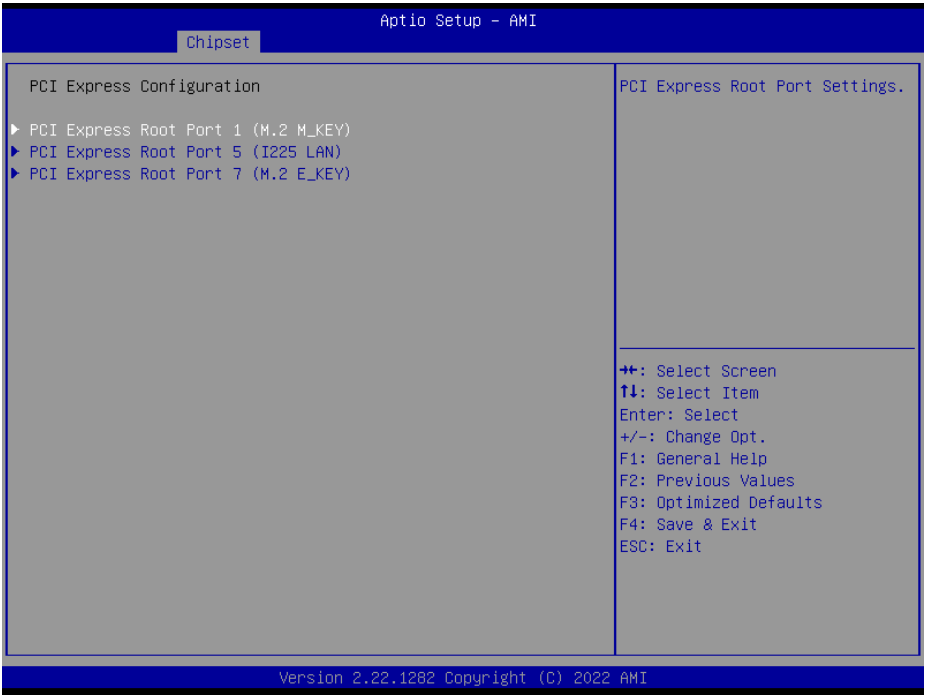


PCH-IO Configuration Screen

BIOS Setting	Options	Description/Purpose
PCI Express Configuration	Sub-Menu	PCI Express Configuration settings.
SATA Configuration	Sub-Menu	SATA Configuration settings.
Restore AC Power Loss	- Power On - Power Off (Default)	Specifies what state to go to when power is re-applied after a power failure (G3 state).
LPC Debug 80 Port	- Disabled (Default) - Enabled	Enables or Disables LPC Debug 80 Port.

PCH-IO Configuration – PCI Express Configuration

Menu Path *Chipset > PCH-IO Configuration > PCI Express Configuration*

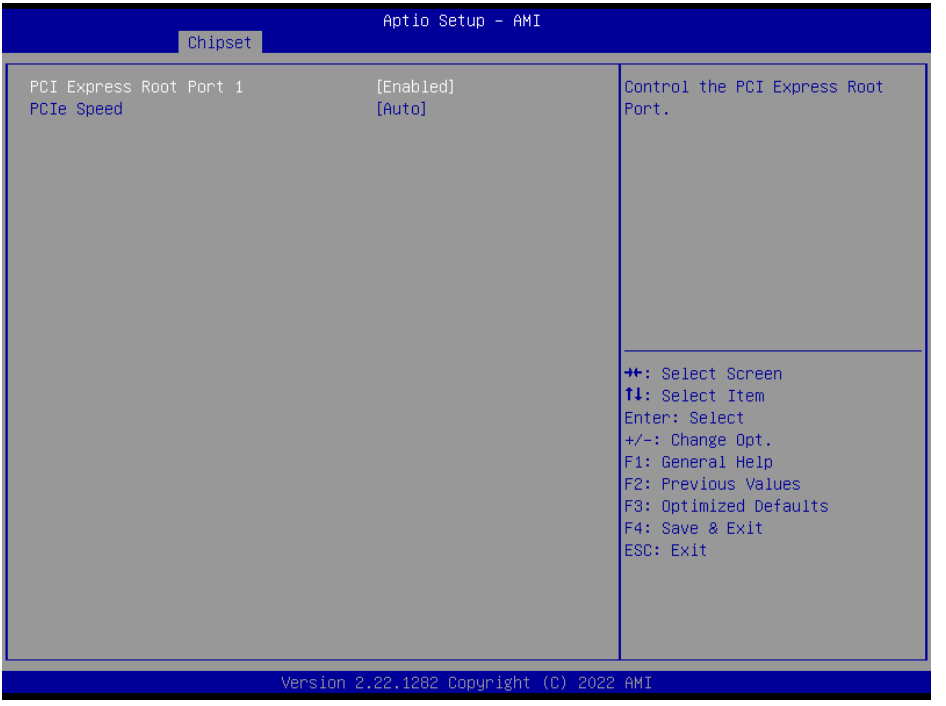


PCI Express Configuration Screen

BIOS Setting	Options	Description/Purpose
PCI Express Root Port 1 (M.2 M_KEY)	Sub-Menu	PCI Express M.2 M_KEY settings.
PCI Express Root Port 5 (I225 LAN)	Sub-Menu	PCI Express I225 LAN settings.
PCI Express Root Port 7 (M.2 E_KEY)	Sub-Menu	PCI Express M.2 E_KEY settings.

PCH-IO Configuration – PCI Express Configuration – PCI Express Root Port 1 (M.2 M_KEY)

Menu Path *Chipset > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port 1 (M.2 M_KEY)*

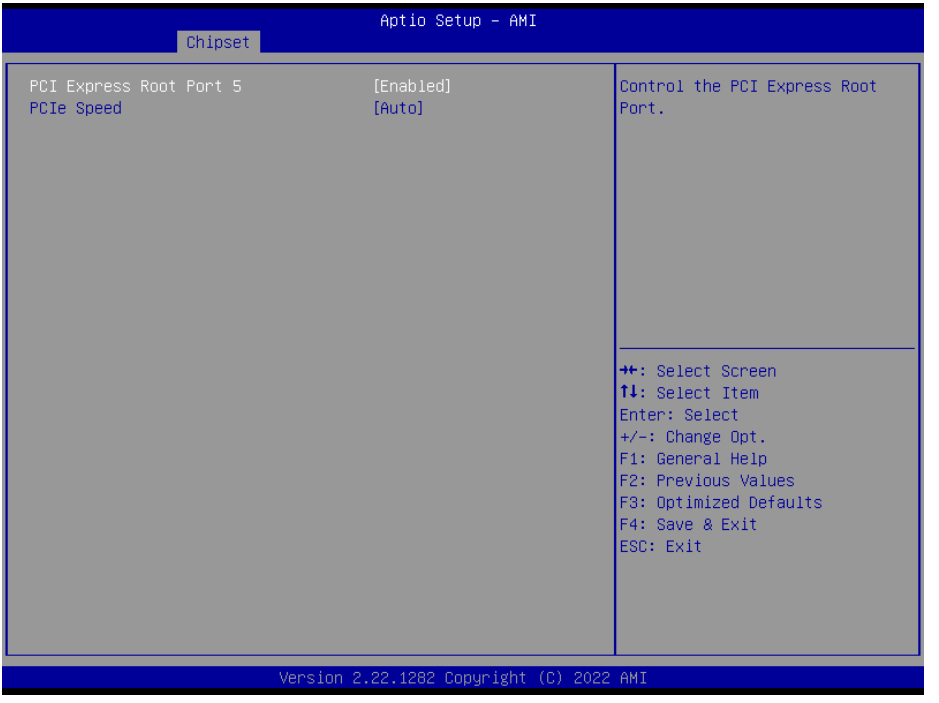


PCI Express Root Port 1 (M.2 M_KEY) Screen

BIOS Setting	Options	Description/Purpose
PCI Express Root Port 1	- Disabled - Enabled (Default)	Enables or Disables the PCI Express Root Port.
PCIe Speed	- Auto (Default) - Gen1 - Gen2 - Gen3	Configures PCIe Speed.

PCH-IO Configuration – PCI Express Configuration – PCI Express Root Port 5 (I225 LAN)

Menu Path *Chipset > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port 5 (I225 LAN)*

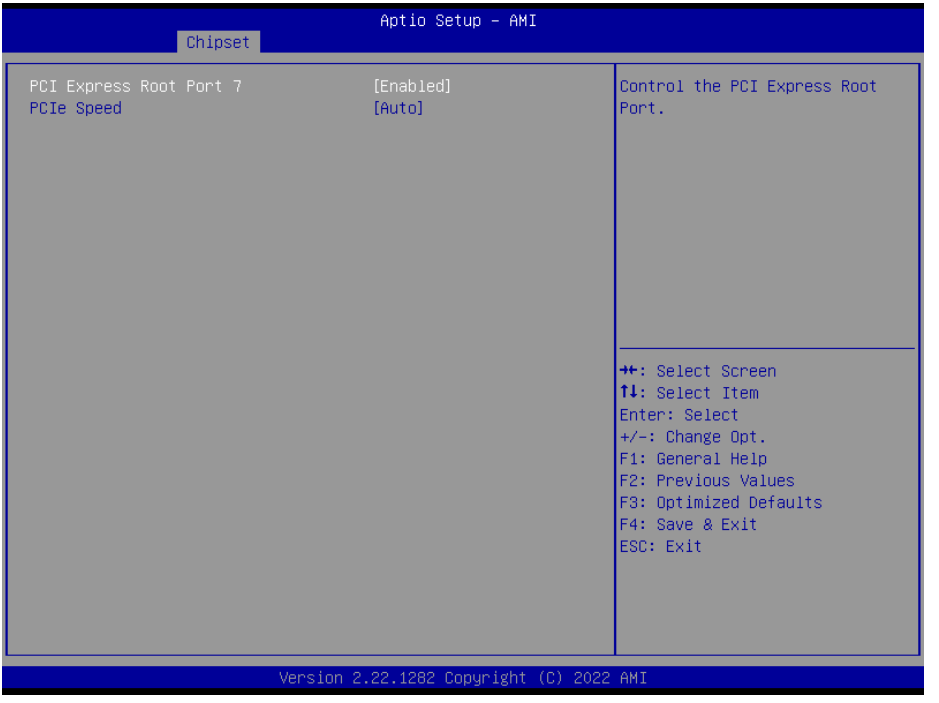


PCI Express Root Port 5 (I225 LAN) Screen

BIOS Setting	Options	Description/Purpose
PCI Express Root Port 5	- Disabled - Enabled (Default)	Enables or Disables the PCI Express Root Port.
PCIe Speed	- Auto (Default) - Gen1 - Gen2 - Gen3	Configures PCIe Speed.

PCH-IO Configuration – PCI Express Configuration – PCI Express Root Port 7 (M.2 E_KEY)

Menu Path *Chipset > PCH-IO Configuration > PCI Express Configuration > PCI Express Root Port 7 (M.2 E_KEY)*

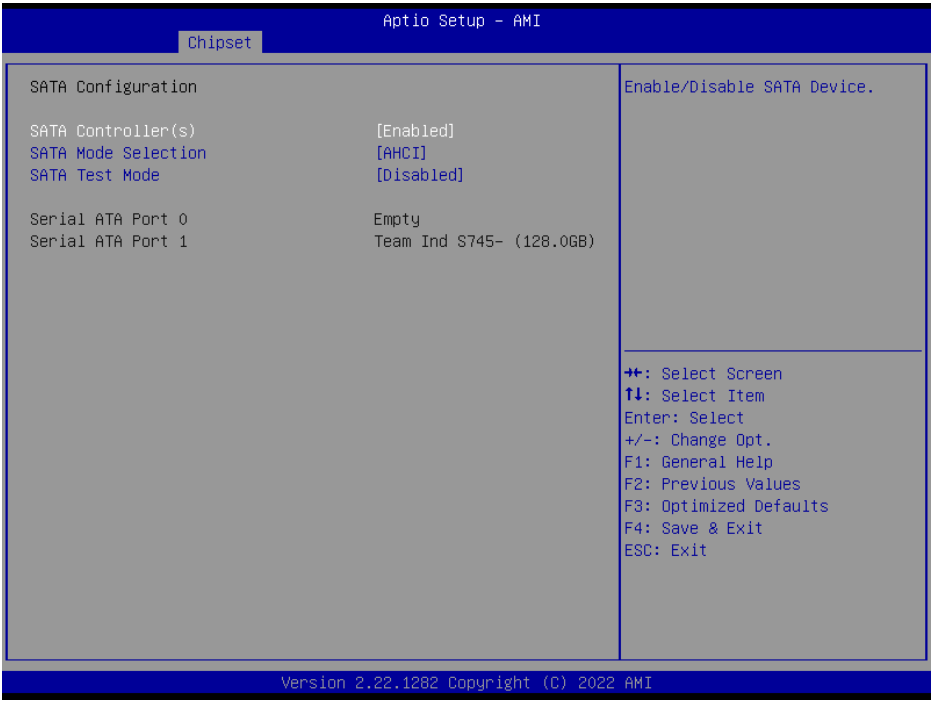


PCI Express Root Port 7 (M.2 E_KEY) Screen

BIOS Setting	Options	Description/Purpose
PCI Express Root Port 7	- Disabled - Enabled (Default)	Enables or Disables the PCI Express Root Port.
PCIe Speed	- Auto (Default) - Gen1 - Gen2 - Gen3	Configures PCIe Speed.

PCH-IO Configuration – SATA Configuration

Menu Path *Chipset > PCH-IO Configuration > SATA Configuration*



SATA Configuration Screen

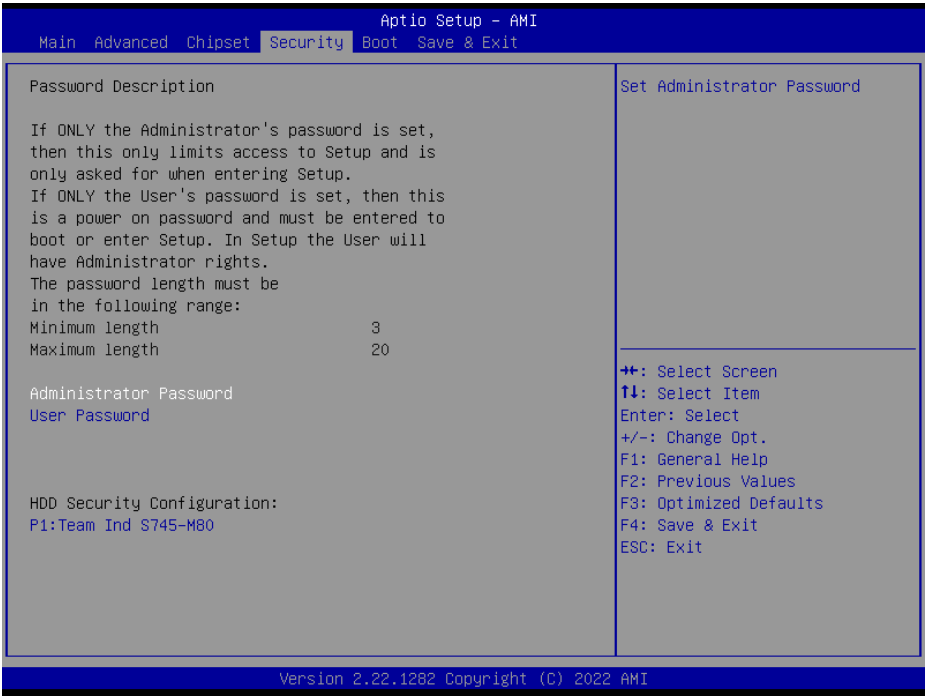
BIOS Setting	Options	Description/Purpose
SATA Controller(s)	- Enabled (Default) - Disabled	Enables or Disables SATA Device.
SATA Mode Selection	- AHCI (Default)	Determines how SATA controller(s) operate.
SATA Test Mode	- Enabled - Disabled (Default)	Enables / Disables SATA Test Mode (For test only)
Serial ATA Port 0~1	No changeable options	Displays the SATA device's name.

5.1.5 Security

Menu Path *Security*

From the **Security** menu, you are allowed to create, change or clear the administrator password. You will be asked to enter the configured administrator password before you can access the Setup Utility.

By setting an administrator password, you will prevent other users from changing your BIOS settings. You can configure an Administrator password and then configure a user password. An administrator has much more privileges over the settings in the Setup utility than a user. Heed that a user password does not provide access to most of the features in the Setup utility.



Security Menu Screen

BIOS Setting	Options	Description/Purpose
Administrator Password	Password can be 3-20 alphanumeric characters.	Specifies the administrator password.
User Password	Password can be 3-20 alphanumeric characters.	Specifies the user password.

BIOS Setting	Options	Description/Purpose
HDD Security Configuration	Sub-Menu	Enters the sub-menu with option to enabled password protected HDD/SSD (if supported by SATA device).

Create an Administrator or User Password

1. Select the **Administrator Password** / **User Password** option from the Security menu and press <Enter>, and the password dialog entry box appears.
2. Enter the password you want to create. A password can be 3-20 alphanumeric characters.
   After you have configured the password, press <Enter> to confirm.
3. Type the new password again and press <Enter>.

Change an Administrator or User Password

1. Select the **Administrator Password** / **User Password** option from the Security menu and press <Enter>, and the password dialog entry box appears.
2. Select the Administrator Password or User Password that you want to change. A password can be 3-20 alphanumeric characters. After you have changed the password, press <Enter> to confirm.
3. Type the changed password again and press <Enter>.

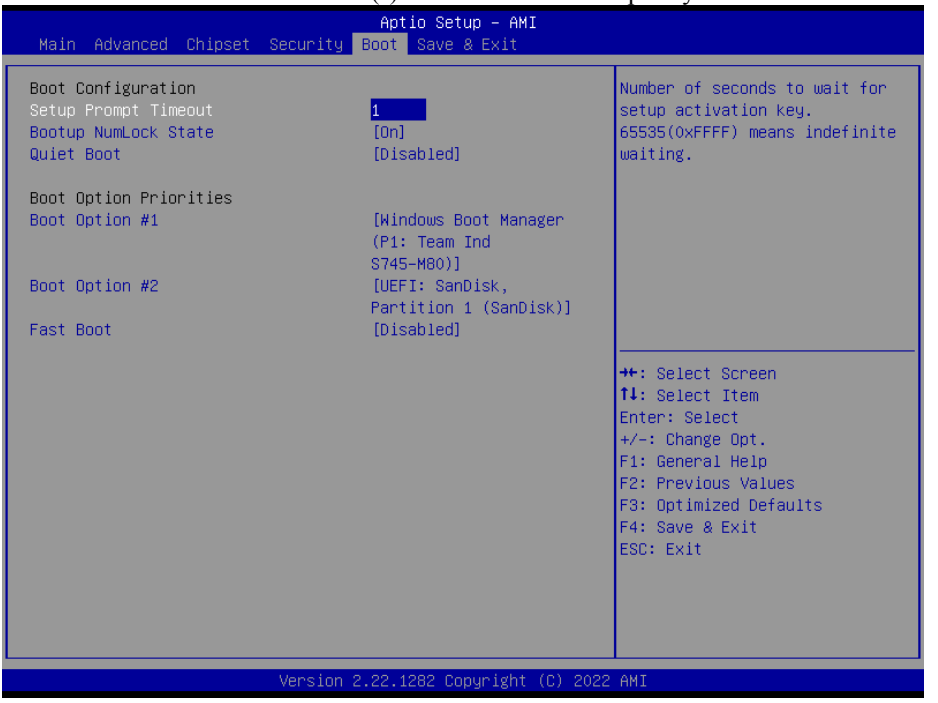
Remove an Administrator or User Password

1. Select the **Administrator Password** / **User Password** option from the Security menu and press <Enter>, and the password dialog entry box appears.
2. Select the configured Administrator Password or User Password that you want to delete.
   Leave the dialog box blank and press <Enter>.
3. Press <Enter> again when the password confirmation box appears.

5.1.6 Boot

Menu Path *Boot*

This menu provides control items for system boot configuration such as setting setup prompt timeout, enabling/disabling quiet boot and fast boot, changing the boot order from the available bootable device(s) and Screen Rotation policy.



Boot Menu Screen

BIOS Setting	Options	Description/Purpose
Setup Prompt Timeout	Numeric (from 1 to 65535)	Number of seconds to wait for setup activation key.
Bootup NumLock State	- On (Default) - Off	Selects the NumLock sate after the system is powered on. • **On:** Enable the NumLock function automatically after the system is powered on. • **Off:** Disable the NumLock function after the system is powered on.
Quiet Boot	- Disabled (Default) - Enabled	Enables or Disables Quiet Boot options.

BIOS Setting	Options	Description/Purpose
Boot Option #1~#n	- [Drive(s)] - Disabled	Sets the system boot order.
Fast Boot	- Disabled (Default) - Enabled	Enables or Disables Fast Boot options.

5.1.7 Save & Exit

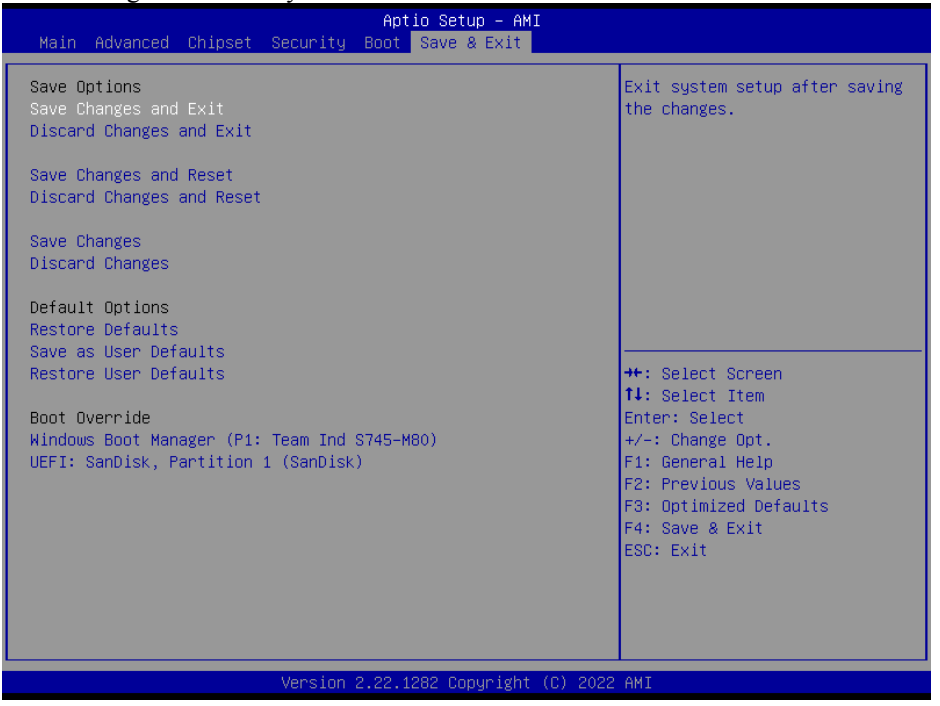
Menu Path *Save & Exit*

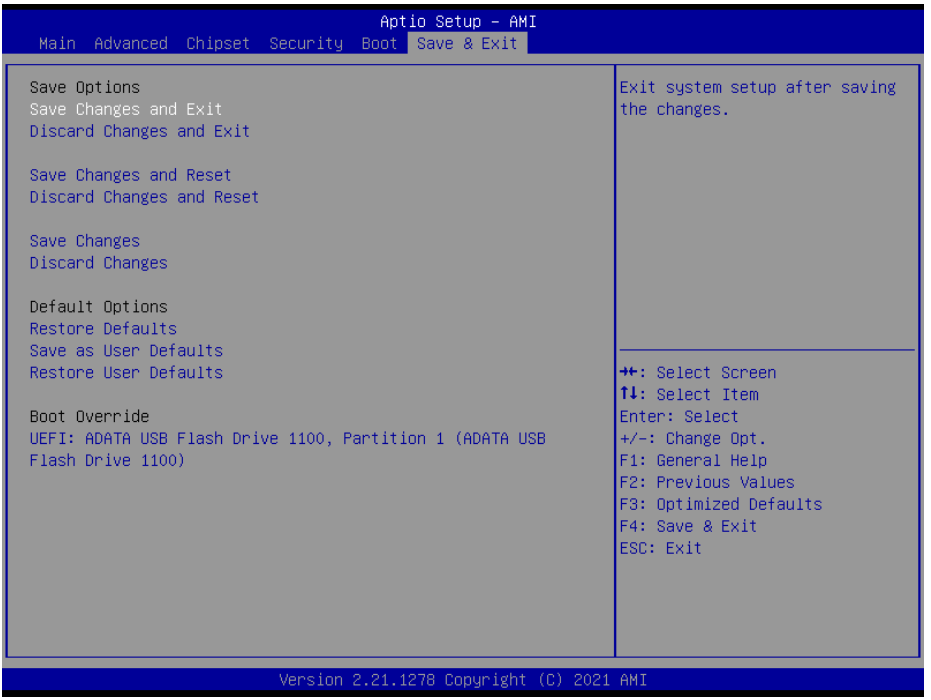
The **Save & Exit** allows users to save or discard changed BIOS settings as well as load factory default settings.

Save Changed BIOS Settings
To save and validate the changed BIOS settings, select **Save Changes** from the **Save & Exit** menu, or you can select **Save Changes and Exit** (or press **F4**) to validate the changes and then exit the system. Select **Save Changes and Reset** to validate the changed BIOS settings and then restart the system

Discard Changed BIOS Settings
To cancel the BIOS settings you have previously configured, select **Discard Changes and Exit** from this menu, or simply press **Esc** to exit the BIOS setup. You can also select **Discard Changes and Reset** to discard any changes you have made and restore the factory BIOS defaults.

Load User Defaults
You may simply press **F3** at any time to load the **Optimized Values** which resets all BIOS settings to the factory defaults.





Save & Exit Menu Screen

BIOS Setting	Options	Description/Purpose
Save Changes and Exit	No changeable options	Exits and saves the changes in NVRAM.
Discard Changes and Exit	No changeable options	Exits without saving any changes made in BIOS settings.
Save Changes and Reset	No changeable options	Saves the changes in NVRAM and resets.
Discard Changes and Reset	No changeable options	Resets without saving any changes made in BIOS settings.
Save Changes	No changeable options	Saves Changes done so far to any of the setup options.
Discard Changes	No changeable options	Discards Changes done so far to any of the setup options.
Restore Defaults	No changeable options	Loads the optimized defaults for BIOS settings.
Save as User Defaults	No changeable options	Saves the changes done so far as User Defaults.
Restore User Defaults	No changeable options	Restores the User Defaults to all the setup options.
Boot Override	- [Drive(s)]	Forces to boot from selected [drive(s)].

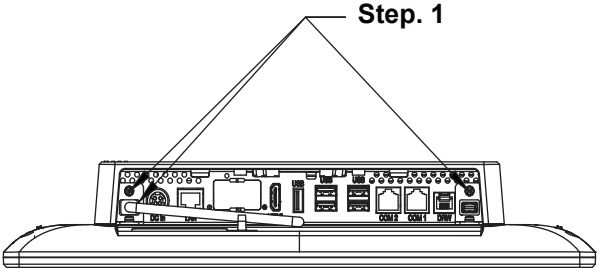
Appendix A System Diagrams

This appendix includes the easy maintenance diagrams, exploded diagrams of the system and the parts list as well as the part numbers of the PA-J501 system.

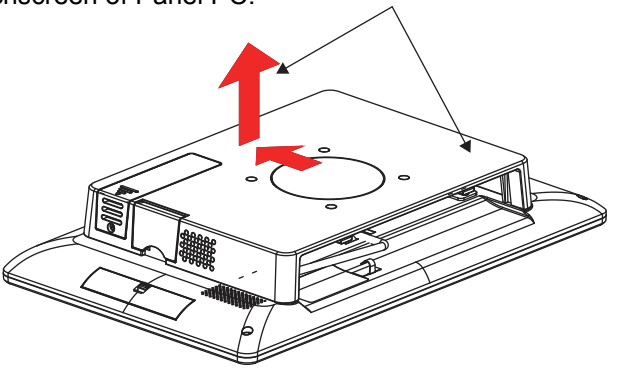
- PPC Memory Maintenance
- PPC M.2 2280 Maintenance
- PA-J501 Memory Maintenance
- PA-J501 M.2 2280 Maintenance
- How To Turn System Touchscreen
- 2nd Display Assembly
- VFD Module Assembly
- iButton Module Assembly
- Fingerprint Module Assembly
- Barcode Scanner Module Assembly
- MSR Module Assembly
- POS Type Assembly Exploded Diagram
- PPC Type Assembly Exploded Diagram

PPC Memory Maintenance

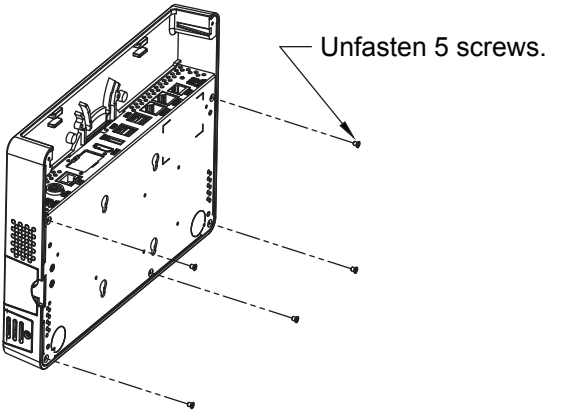
Step 1: Release the 2 screws and unplug the DP cable from the I/O Ports.



Step 2: Follow the directions (red arrows) below to separate the PCB Box from the touchscreen of Panel PC.

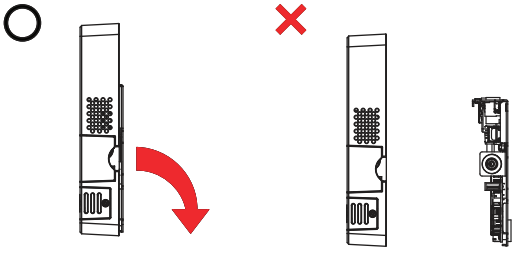


Step 3: Unfasten 5 screws as shown:



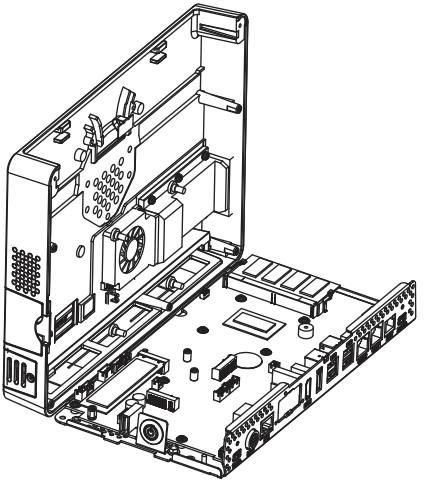
(continued on the next page)

Step 4: Move the PCB box outwards slightly as shown (red arrow) and lay the PCB box down on a flat surface.



Warning: If you force to move the PCB Box too far away from PPC, the connected cables inside could be damaged.

Step 5: Open the cover and unplug all the connected cables.

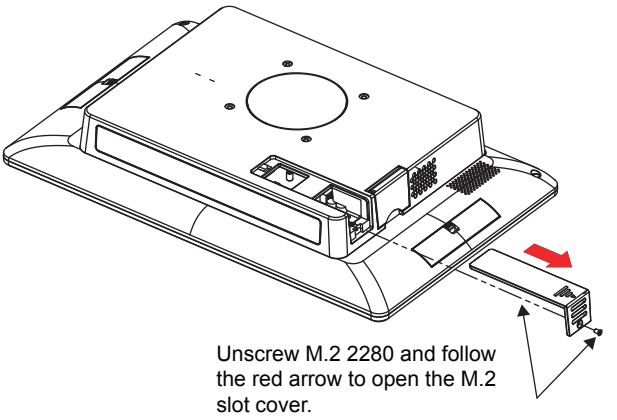


Step 6: Change the memory and heating pad.

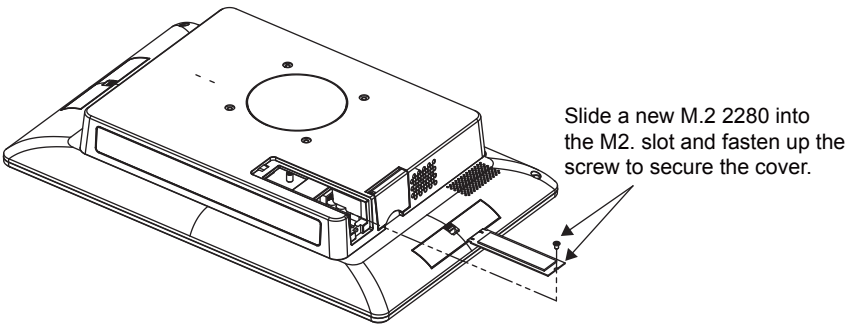
Step 7: Re-connect all the unplugged cables and replace all removed screws in the order you dismantled and complete.

PPC M.2 2280 Maintenance

Step 1: Unscrew M.2 2280 and follow the direction (red arrow) to release the cover.



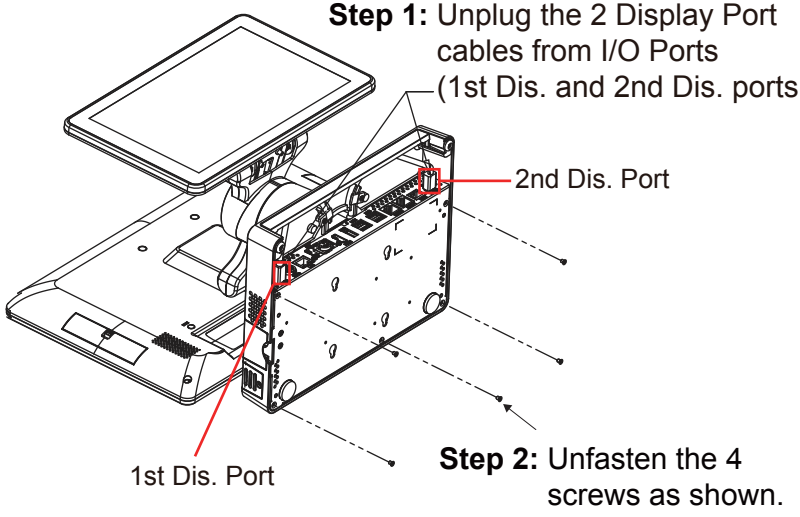
Step 2: Slide a new M.2 2280 into the M2. slot and fasten up the screw to secure the cover and complete.



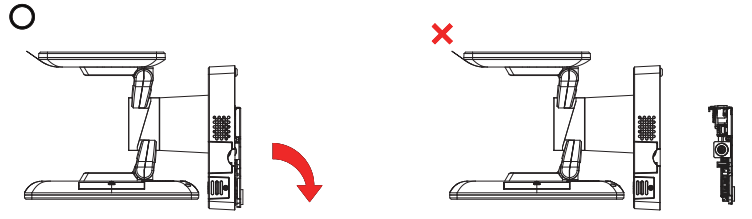
PA-J501 Memory Maintenance

Step 1: Unplug the 2 Display Port cables from I/O Ports (1st Dis. and 2nd Dis. ports).

Step 2: Unfasten the 4 screws as shown:

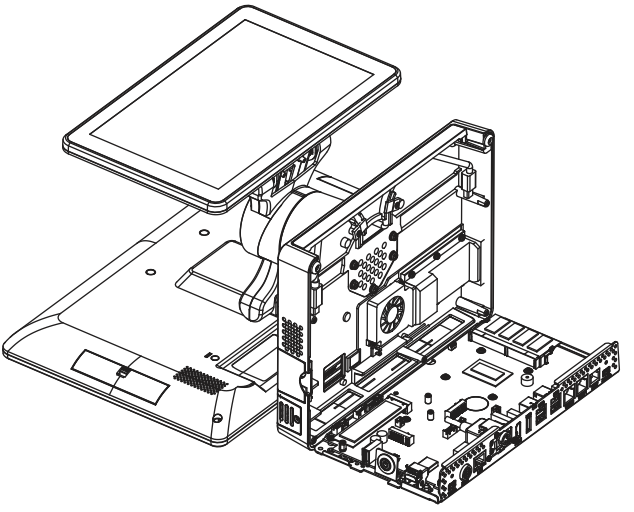


Step 3: Move the PCB box outwards slightly as shown (red arrow) and lay the PCB box down on a flat surface.



Warning: If you force to move the PCB Box too far away from the POS system, the connected cables inside the system could be damaged.

Step 4: Open the cover and unplug all the connected cables. (Remove the LED cable and Wi-Fi antenna if Wi-Fi function is available.)



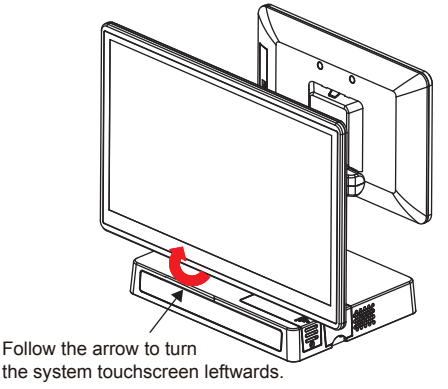
Step 5: Change the memory and heating pad.

Step 6: Re-connect all the unplugged cables and replace all removed screws in the order you dismantled.

The memory replacement has been finished.

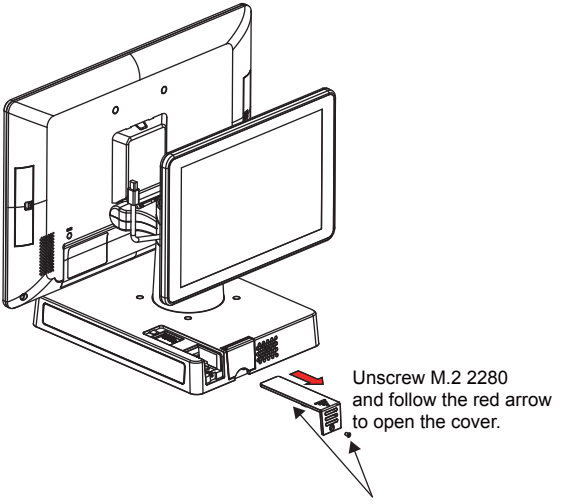
PA-J501 M.2 2280 Maintenance

Step 1: Follow the orange arrow to turn the system touchscreen leftwards.



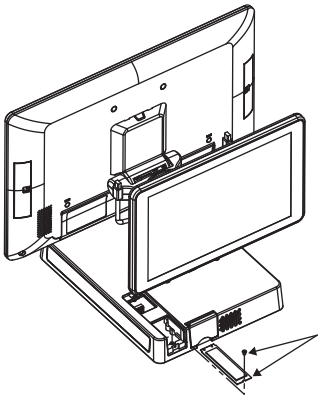
Note: Please refer to the **"How To Turn System Touchscreen"** section on the next page on how to turn the primary touchscreen properly.

Step 2: Unscrew M.2 2280 and follow the direction of red arrow (as shown) to release the cover.



(continued on the next page)

Step 3: Slide a new M.2 2280 into the M2. slot and fasten up the screw to secure the cover and complete.

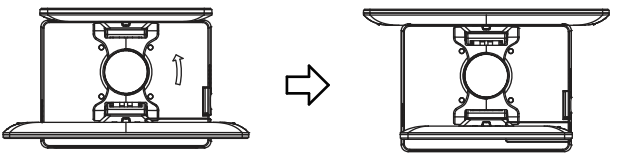


Slide a new M.2 2280 into the M2. slot and fasten up the screw to secure the cover.

How To Turn System Touchscreen

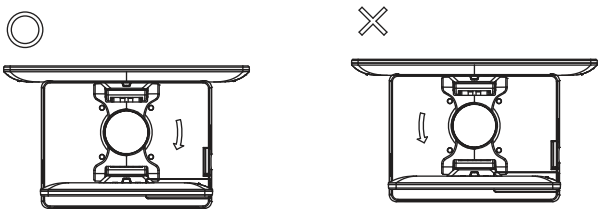
You can turn the POS touchscreen either way. Heed that after you turn the primary touchscreen to the rear side, you must turn the primary touchscreen only in the direction you previously turned.

PA-J501 System Top View



In this example, the primary touchscreen is to be turned leftwards.

The primary touchscreen has been turned as illustrated.



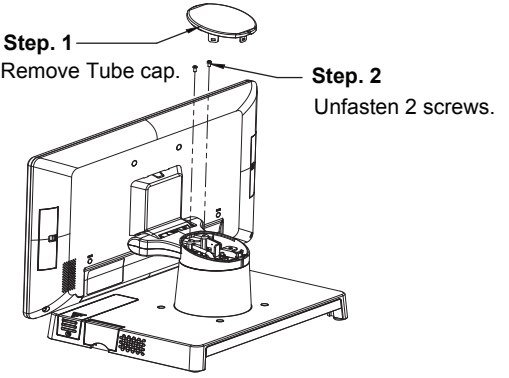
Important: Please turn the primary touchscreen only in the direction you previously turned.

Warning: If you force to turn not in the direction you previously turned, the internal structure of the POS system could be damaged.

2nd Display Assembly

Step 1: Remove Tube Cap.

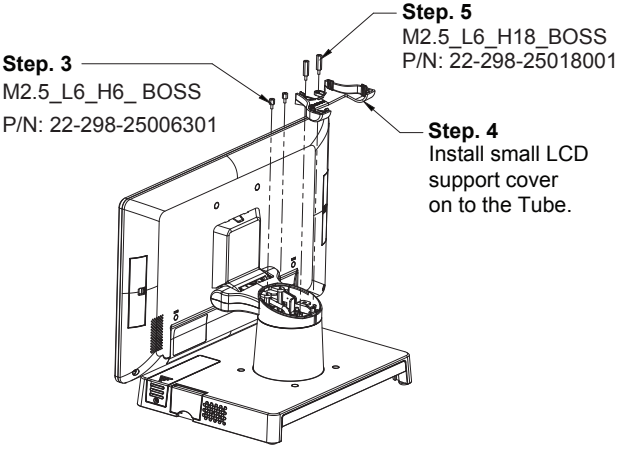
Step 2: Unfasten the 2 screws as shown:



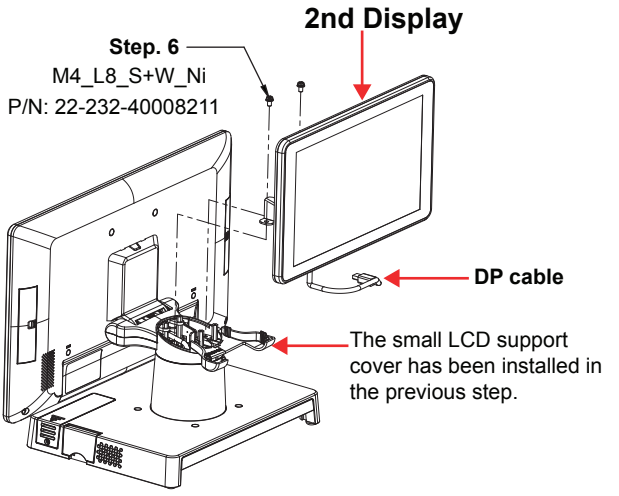
Step 3: Fasten 2 HEX CU BOSS (P/N: 22-298-25006301) as shown:

Step 4: Install the small LCD support cover onto Tube.

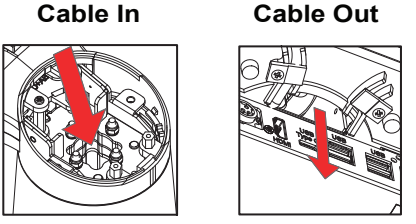
Step 5: Fasten the 2 HEX CU BOSS (P/N: 22-298-25018001) to secure the small LCD support cover onto the Tube.



Step 6: Fasten the 2 screws (P/N: 22-232-40008211) and install 2nd Display onto the back of PA-J501 Panel PC.



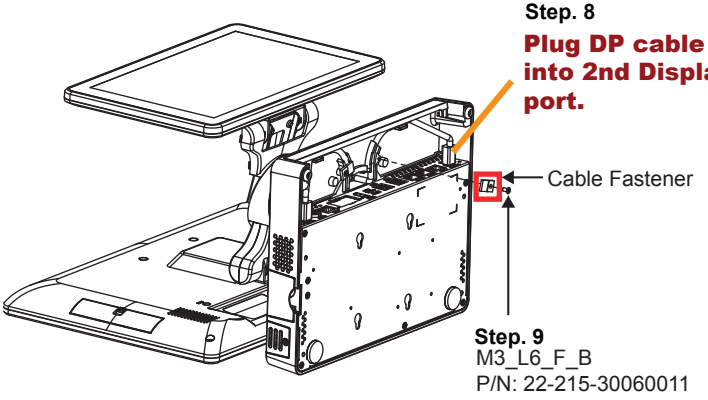
Step 7: Wire DP cable into the Tube as shown and out from the top side of rear I/O panel as illustrated below:



(continued on the next page)

Step 8: Plug DP cable into the 2nd Display port on the rear I/O panel as shown:

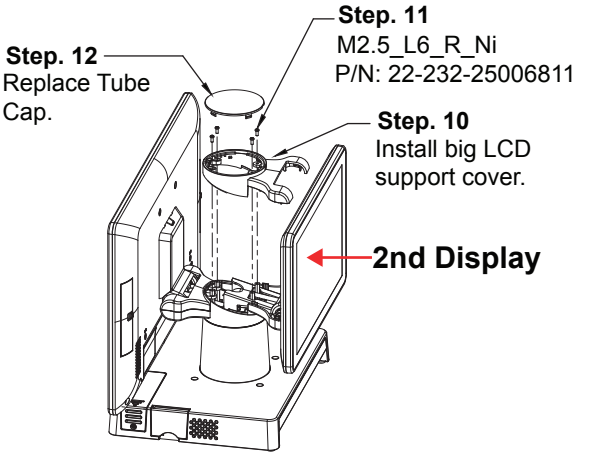
Step 9: Install the screw (P/N: 22-215-30060011) to attach the cable fastener.



Step 10: Install the big LCD small support cover onto the Tube.

Step 11: Fasten 4 screws (P/N: 22-232-25006811) to secure big LCD small support cover. Note 2 screws in Step 2 are used in this step.

Step 12: Replace Tube Cap to finish the 2nd Display assembly.

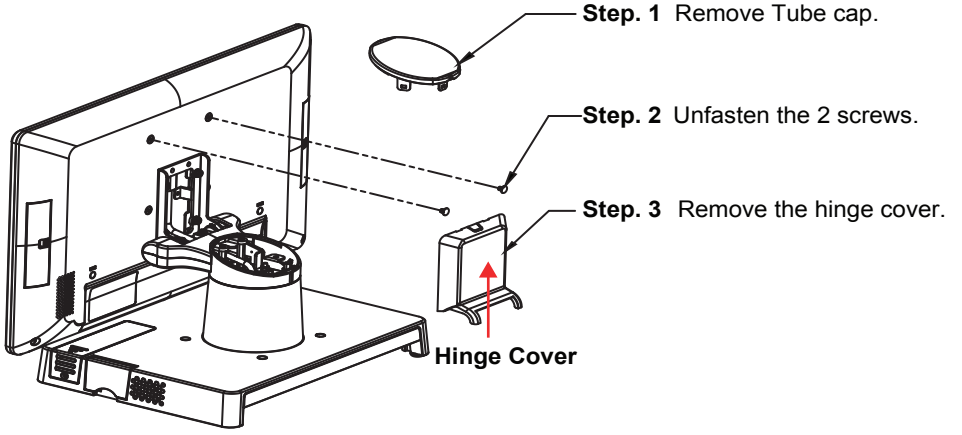


VFD Module Assembly

Step 1: Remove Tube Cap.

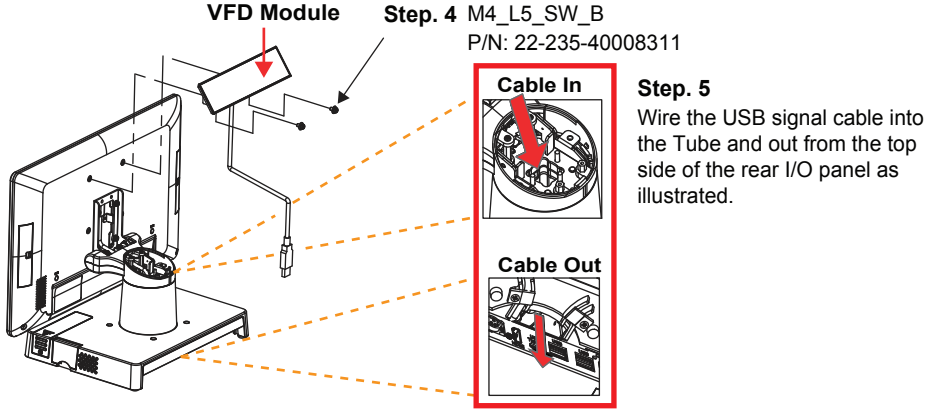
Step 2: Unfasten the 2 screws as shown:

Step 3: Remove the Hinge Cover.



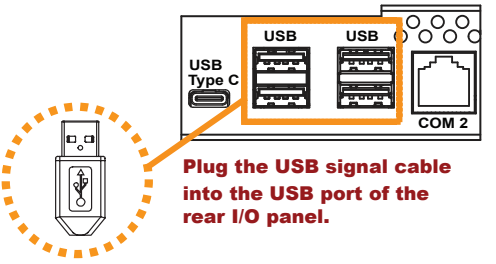
Step 4: Tighten 2 screws (P/N: 22-235-40008311) to fix VFD module onto the rear of Panel PC.

Step 5: Wire the USB signal cable into the Tube as shown and out from the top side of the rear I/O panel as illustrated below:

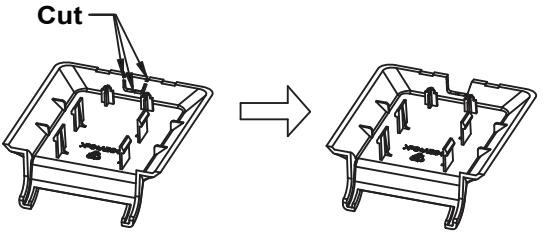


(continued on the next page)

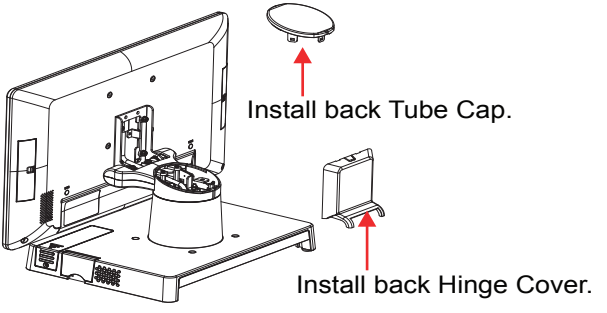
Step 6: Plug the USB signal cable into the USB port on the rear I/O panel as shown below:



Step 7: Cut the pieces of Hinge Cover as shown to allow the cable to wire through.

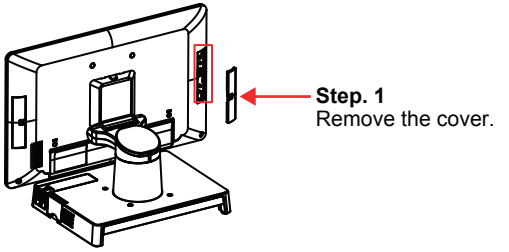


Step 8: Replace Tube Cap and Hinge Cover to finish the assembly.

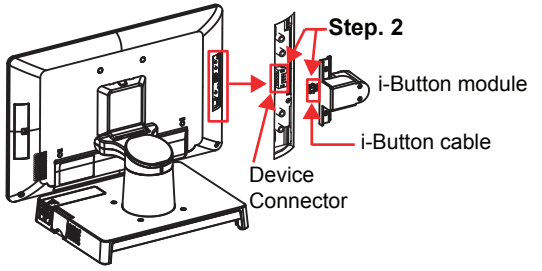


iButton Module Assembly

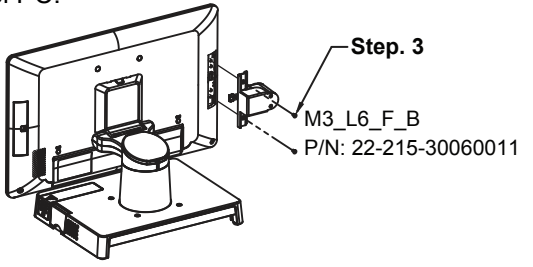
Step 1: Remove the Cover as shown:



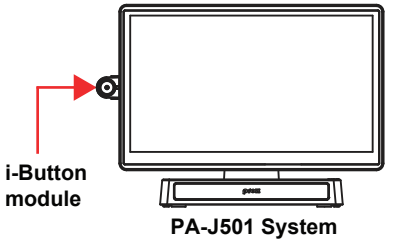
Step 2: Connect i-Button cable with the device connector as shown:



Step 3: Fasten 2 screws (P/N: 22-215-30060011) to secure i-Button device onto Panel PC.

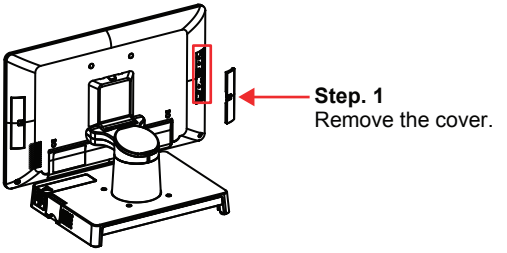


The i-Button module assembly has been finished as below:

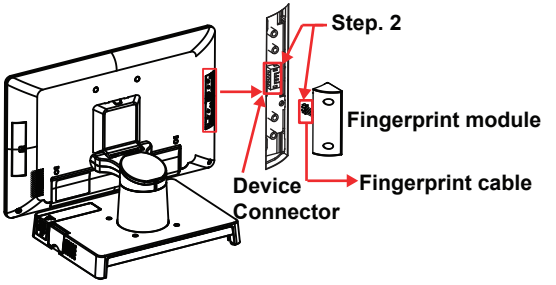


Fingerprint Module Assembly

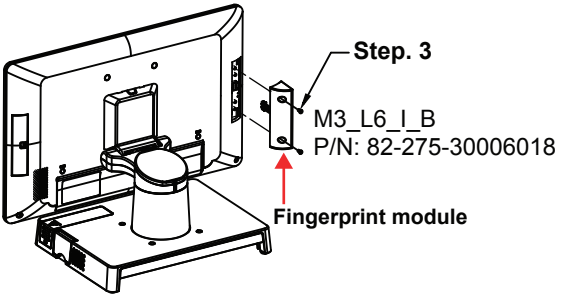
Step 1: Remove the Cover as shown:



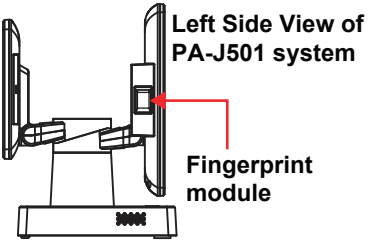
Step 2: Connect Fingerprint cable with the device connector as shown:



Step 3: Tighten 2 screws (P/N: 82-275-30006018) to secure Fingerprint module onto Panel PC.

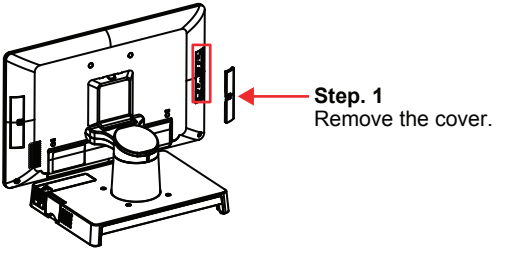


The Fingerprint module assembly has been finished as below:

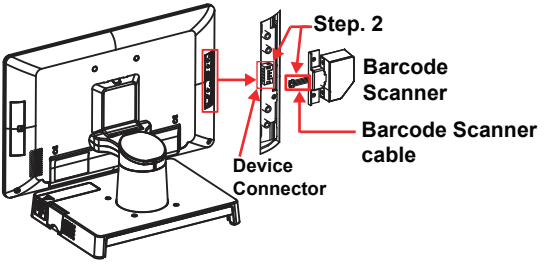


Barcode Scanner Assembly

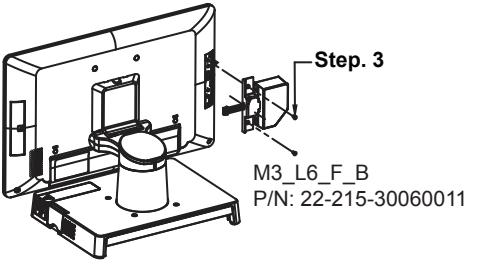
Step 1: Remove the Cover as shown:



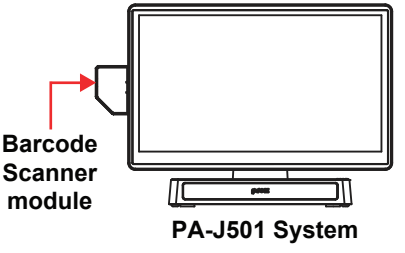
Step 2: Connect Barcode Scanner cable with the device connector as shown:



Step 3: Fasten 2 screws (P/N: 22-215-30060011) to secure Barcode Scanner onto Panel PC.

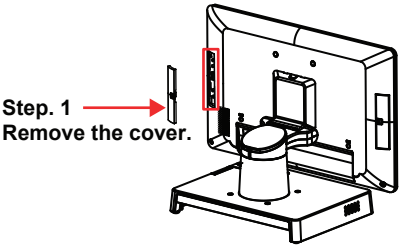


The Barcode Scanner assembly has been finished as below:

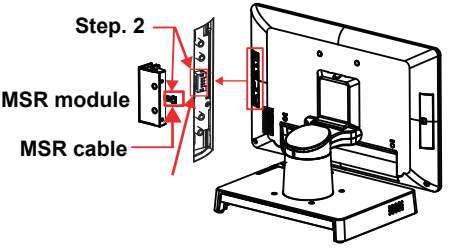


MSR Module Assembly

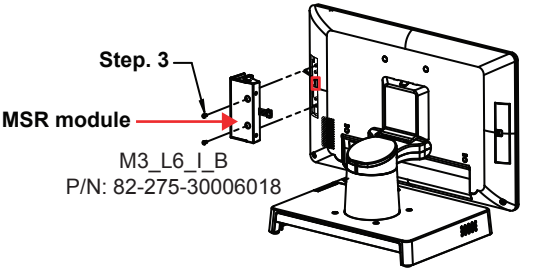
Step 1: Remove the Cover as shown:



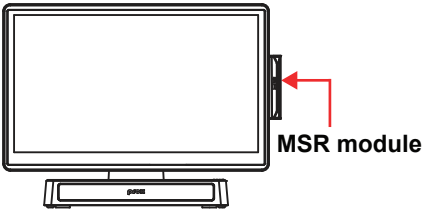
Step 2: Connect MSR cable with the device connector as shown:



Step 3: Tighten 2 screws (P/N: 82-275-30006018) to secure MSR module onto Panel PC.

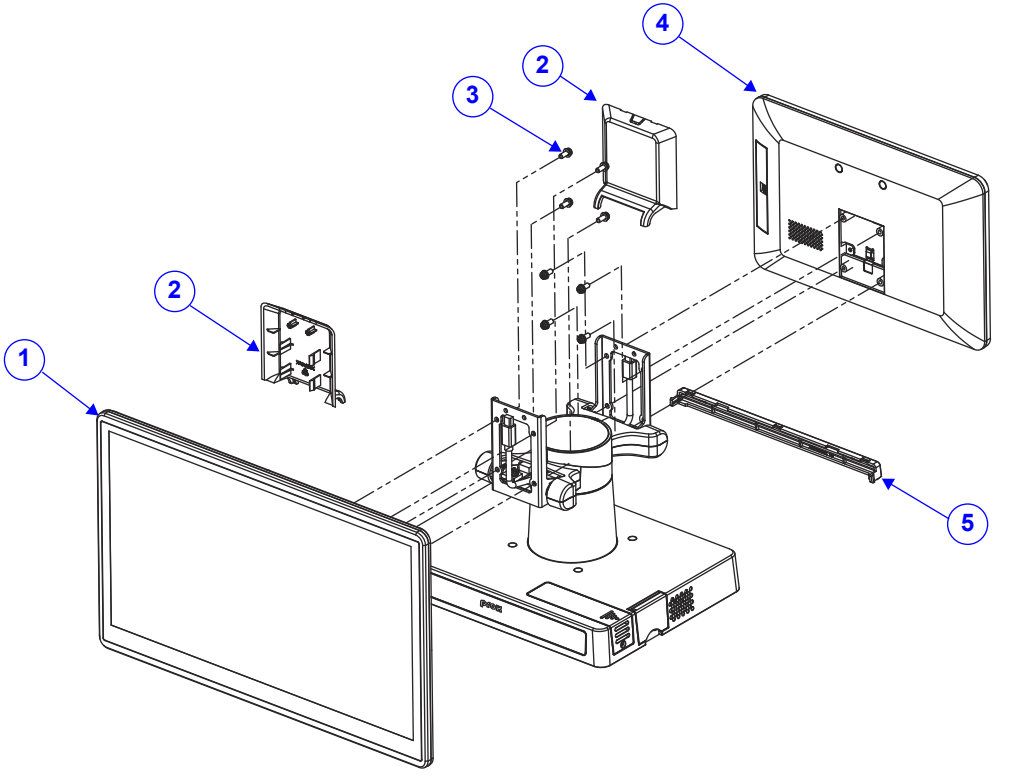


The MSR module assembly has been finished as below:



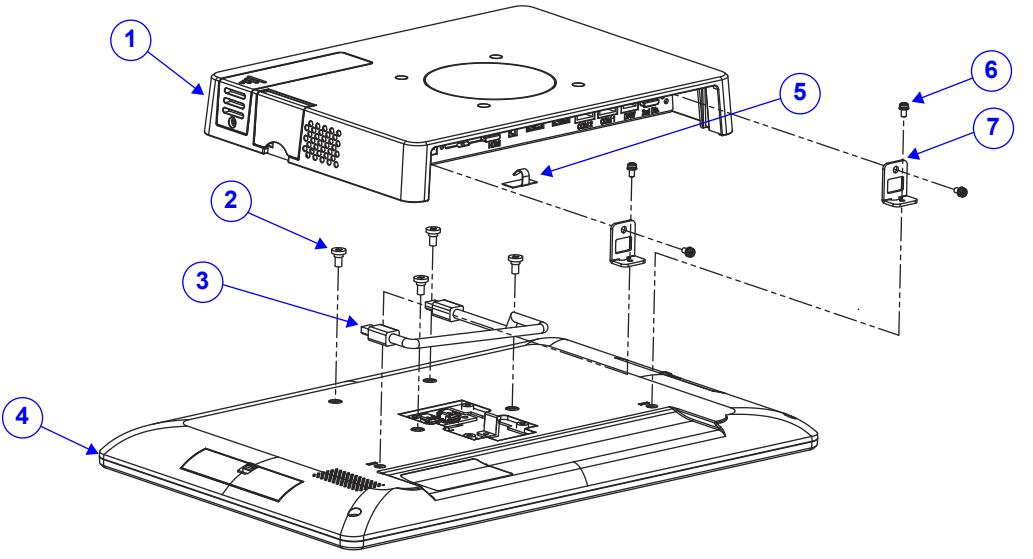
PA-J501 System

POS Type Assembly Exploded Diagram



No.	Component Name	P/N No.	Q'ty
1	15.6" LCD	N/A	1
2	PA-J501 Hinge Cover (Black)	30-002-12210514	2
3	Round Head With Spring Washer Screw #2 / M4x0.7Px10mm	22-232-40010011	13
4	PA-J200 2nd Display	N/A	1
5	PA-J500 Cable Cover (Black)	30-002-12110514	1

PPC Type Assembly Exploded Diagram



No.	Component Name	P/N No.	Q'ty
1	PA-J501 PPC Box ASM	N/A	1
2	Fillister Head Screw #2 / M4x0.7Px6mm	22-272-40006911	4
3	Mini DP Cable (L=270mm)	27-072-51405111	1
4	15.6" LCD	N/A	1
5	Locking Cable Clamp	30-042-32100000	1
6	Round Head With Spring Washer Screw M3x0.5Px6mm	22-232-30060211	4
7	PA-J501 Box Fix	20-040-03002514	2

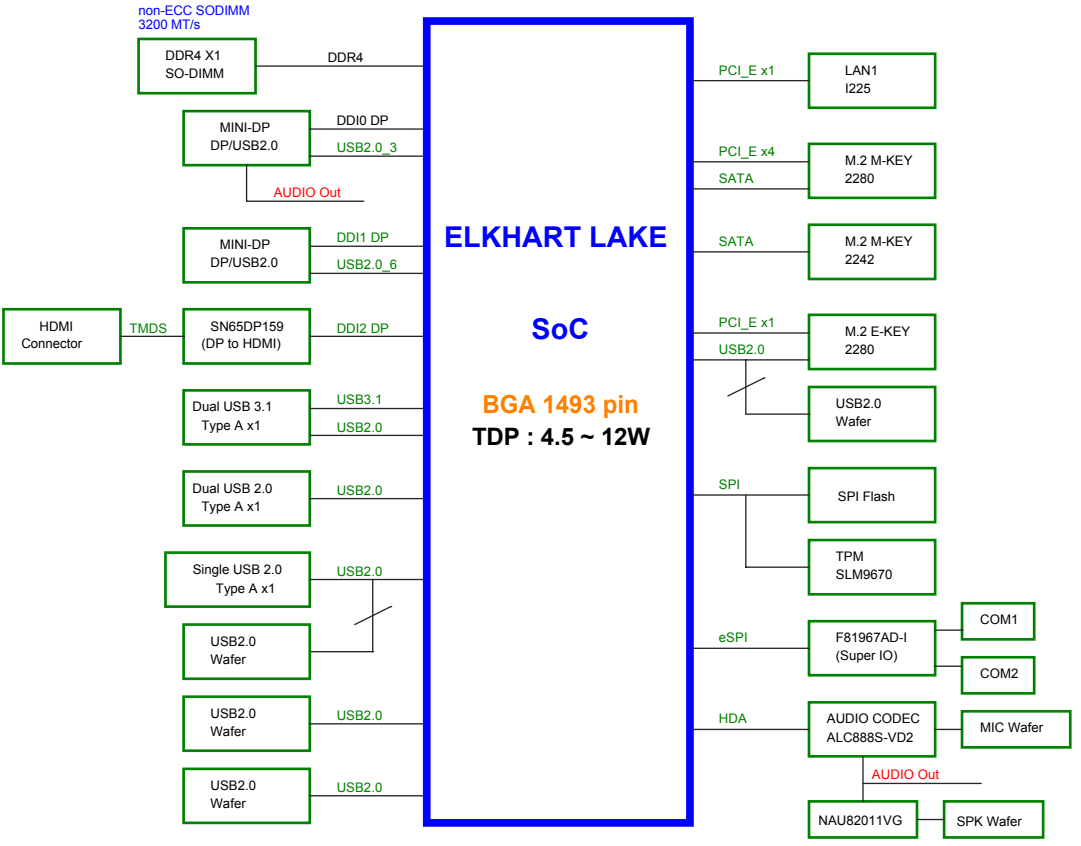
Appendix B Technical Summary

This appendix will give you a brief introduction of the allocation maps for the system resources.

The following topics are included:

- Block Diagram
- Interrupt Map
- I/O Map
- Memory Map
- Configuring WatchDog Timer
- Flash BIOS Update

Block Diagram



Interrupt Map

IRQ	Assignment
IRQ 0	System timer
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 7	Communications Port (COM3)
IRQ 8	System CMOS/real time clock
IRQ 10	Communications Port (COM4)
IRQ 14	Motherboard resources
IRQ 16	High Definition Audio Controller
IRQ 54	Microsoft ACPI-Compliant System
IRQ 55	Microsoft ACPI-Compliant System
IRQ 56	Microsoft ACPI-Compliant System
IRQ 57	Microsoft ACPI-Compliant System
IRQ 58	Microsoft ACPI-Compliant System
IRQ 59	Microsoft ACPI-Compliant System
IRQ 60	Microsoft ACPI-Compliant System
IRQ 61	Microsoft ACPI-Compliant System
IRQ 62	Microsoft ACPI-Compliant System
IRQ 63	Microsoft ACPI-Compliant System
IRQ 64	Microsoft ACPI-Compliant System
IRQ 65	Microsoft ACPI-Compliant System
IRQ 66	Microsoft ACPI-Compliant System
IRQ 67	Microsoft ACPI-Compliant System
IRQ 68	Microsoft ACPI-Compliant System
IRQ 69	Microsoft ACPI-Compliant System
IRQ 70	Microsoft ACPI-Compliant System
IRQ 71	Microsoft ACPI-Compliant System
IRQ 72	Microsoft ACPI-Compliant System
IRQ 73	Microsoft ACPI-Compliant System
IRQ 74	Microsoft ACPI-Compliant System

IRQ	Assignment
IRQ 75	Microsoft ACPI-Compliant System
IRQ 76	Microsoft ACPI-Compliant System
IRQ 77	Microsoft ACPI-Compliant System
IRQ 78	Microsoft ACPI-Compliant System
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IRQ	Assignment
IRQ 105	Microsoft ACPI-Compliant System
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IRQ	Assignment
IRQ 135	Microsoft ACPI-Compliant System
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ	Assignment
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IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967286	Intel(R) Management Engine Interface #1
IRQ 4294967287	Intel(R) Ethernet Controller (3) I225-LM
IRQ 4294967288	Intel(R) Ethernet Controller (3) I225-LM
IRQ 4294967289	Intel(R) Ethernet Controller (3) I225-LM

IRQ	Assignment
IRQ 4294967290	Intel(R) Ethernet Controller (3) I225-LM
IRQ 4294967291	Intel(R) Ethernet Controller (3) I225-LM
IRQ 4294967292	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967293	Intel(R) UHD Graphics
IRQ 4294967294	Standard SATA AHCI Controller

Note: These resource information were gathered using Windows 10.
(The IRQ could be assigned differently depending on OS)

I/O MAP

I/O Map	Assignment
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x0000002E-0x0000002F	Motherboard resources
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x00000040-0x00000043	System timer
0x0000004E-0x0000004F	Motherboard resources
0x00000050-0x00000053	System timer
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller

I/O Map	Assignment
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B2-0x000000B3	Motherboard resources
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000002E8-0x000002EF	Communications Port (COM4)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000003F8-0x000003FF	Communications Port (COM1)
0x000004D0-0x000004D1	Programmable interrupt controller
0x00000680-0x0000069F	Motherboard resources
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x0000164E-0x0000164F	Motherboard resources
0x00001800-0x000018FE	Motherboard resources
0x00001854-0x00001857	Motherboard resources
0x00002000-0x000020FE	Motherboard resources
0x00003000-0x00003FFF	Intel(R) PCI Express Root Port #0 - 4B38
0x00004000-0x0000403F	Intel(R) UHD Graphics
0x00004060-0x0000407F	Standard SATA AHCI Controller
0x00004080-0x00004083	Standard SATA AHCI Controller
0x00004090-0x00004097	Standard SATA AHCI Controller
0x0000EFA0-0x0000EFBF	Intel(R) SMBus Controller - 4B23

Memory Map

Memory Map	Assignment
0xFEC80000-0xFECFFFFF	Motherboard resources
0xFEDA0000-0xFEDA0FFF	Motherboard resources
0xFEDA1000-0xFEDA1FFF	Motherboard resources
0xC0000000-0xCFFFFFFF	Motherboard resources
0xFED20000-0xFED7FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xFFEFC000-0xFFEFFFFF	High Definition Audio Controller
0xFFF00000-0xFFFFFFFF	High Definition Audio Controller
0x80600000-0x807FFFFF	Intel(R) PCI Express Root Port #4 - 4B3C
0x80600000-0x807FFFFF	Intel(R) Ethernet Controller (3) I225-LM
0xFED00000-0xFED003FF	High precision event timer
0x0000-0x9FFFFF	Intel(R) PCI Express Root Port #0 - 4B38
0xFE010000-0xFE010FFF	Intel(R) SPI (flash) Controller - 4B24
0xFD000000-0xFD68FFFF	Motherboard resources
0xFD6F0000-0xFDFFFFFF	Motherboard resources
0xFE000000-0xFE01FFFF	Motherboard resources
0xFE200000-0xFE7FFFFF	Motherboard resources
0xFF000000-0xFFFFFFFF	Motherboard resources
0xFD6B0000-0xFD6CFFFF	Motherboard resources
0xFD6B0000-0xFD6CFFFF	Motherboard resources
0x80800000-0x80801FFF	Standard SATA AHCI Controller
0x80803000-0x808030FF	Standard SATA AHCI Controller
0x80802000-0x808027FF	Standard SATA AHCI Controller

Memory Map	Assignment
0x2100000-0x210FFFF	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
0x80700000-0x80703FFF	Intel(R) Ethernet Controller (3) I225-LM
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0x2118000-0x21180FF	Intel(R) SMBus Controller - 4B23
0xFFEFB000-0xFFEFBFFF	Intel(R) Management Engine Interface #1
0x1000000-0x1FFFFFF	Intel(R) UHD Graphics
0x0000-0xFFFFFFF	Intel(R) UHD Graphics
0xFD6E0000-0xFD6EFFFF	Motherboard resources
0xFD6D0000-0xFD6DFFFF	Motherboard resources
0xFD6A0000-0xFD6AFFFF	Motherboard resources
0xFD690000-0xFD69FFFF	Motherboard resources
0xA0000-0xBFFFF	PCI Express Root Complex
0xE0000-0xE3FFF	PCI Express Root Complex
0xE4000-0xE7FFF	PCI Express Root Complex
0xE8000-0xEBFFF	PCI Express Root Complex
0xEC000-0xEFFFF	PCI Express Root Complex
0xF0000-0xFFFFF	PCI Express Root Complex
0x7FC00000-0x805FFFFF	Intel(R) PCI Express Root Port #0 - 4B38
0x7FC00000-0x805FFFFF	PCI Express Root Complex

Configuring WatchDog Timer

The I/O port address of the watchdog timer is 2E (hex) and 2F (hex). 2E (hex) is the address port. 2F (hex) is the data port. User must first assign the address of register by writing address value into address port 2E (hex), then write/read data to/from the assigned register through data port 2F (hex).

Configuration Sequence

To program F81967 configuration registers, the following configuration sequence must be followed:

(1) Enter the extended function mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

(2) Configure the configuration registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1). First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required. Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

(3) Exit the extended function mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

Code example for watch dog timer

Enable watchdog timer and set timeout interval to 30 seconds.

```
; ------------------------ Enter to extended function mode -----------------------------
mov         dx,     2Eh
mov   al,   87h
out   dx,   al
out   dx,   al
; ---------------------- Select Logical Device 7 of watchdog timer ---------------------
mov   al,   07h
out   dx,   al
inc   dx
mov         al,     07h
out   dx,   al
;-------------------------------Enable Watch dog feature ----------------------------
dec   dx
mov         al,     30h
out         dx,     al
inc   dx
mov   al,   01h
out   dx,   al
; ---------------- Set timeout interval as 30seconds and start counting --------------
dec   dx
mov   al,   F6h
out   dx,   al
inc   dx
mov   al,   1Eh
out         dx,     al
;------------------------------ Enable Watch PME-----------------------------------------
dec   dx
mov         al,     FAh
out   dx,   al
inc   dx
in    al,   dx
or    al,   51h
out   dx,   al
;------------------------- Set second as counting unit ------------------------------------
dec   dx
mov   al,   F5h
out   dx,   al
inc   dx
in    al,   dx
and   al,   DEh
out   dx,   al
;------------------------- Start the watchdog timer ---------------------------------
or    al,   20h
out   dx,   al
;--------------------------------Exit the extended function mode ------------------------
dec   dx
mov         al,     AAh
out   dx,   al
```

Cash Drawer CONFIGURATION

The I/O port address is 2E (hex) and 2F (hex). 2E (hex) is the address port. 2F (hex) is the data port. User must first assign the address of register by writing address value into address port 2E (hex), then write/read data to/from the assigned register through data port 2F (hex).

SIO Address	
Cash drawer Open	LDN06, 0x81, bit1
Cash drawer Status	LDN06, 0x81, bit0

Configuration Sequence

To program F81967 configuration registers, the following configuration sequence must be followed:

(1) Enter the extended function mode
To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

(2) Configure the configuration registers
The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1). First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required. Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

(3) Exit the extended function mode
To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

Code example for opening the cash drawer

```
; ------------------------ Enter to extended function mode -----------------------------
mov     dx,  2Eh
mov     al,  87h
out     dx,  al
out     dx,  al
; ---------------------- Select Logical Device 6 of Cash Drawer ---------------------
mov     al,  07h
out     dx,  al
inc     dx
mov     al,  06h
out     dx,  al
;-------------------------------Open the Cash Drawer -----------------------------
mov     al,  81h
out     dx,  al
inc     dx
in      al,   dx
or      al,  02h
out     dx,  al
;-------------------------------Close the Cash Drawer -----------------------------
mov     al,  81h
out     dx,  al
inc     dx
in      al,   dx
and     al,  FDh
out     dx,  al
;-------------------------------Exit the extended function mode ------------------------
dec     dx
mov     al,  AAh
out     dx,  al
```

Flash BIOS Update

I. Prerequisites

1 Prepare a bootable media (e.g. USB storage device) which can boot system to EFI Shell. Note: Copy UEFI Shell into the storage device under specific directory path. (/efi/boot/bootx64.efi)

2 Download and save the BIOS file (e.g. J5010PX1.bin) to the storage device.

3 Copy AMI flash utility – AfuEfix64.efi (v5.14.01.0015) into the storage device. The utility and BIOS file should be saved to the same path.

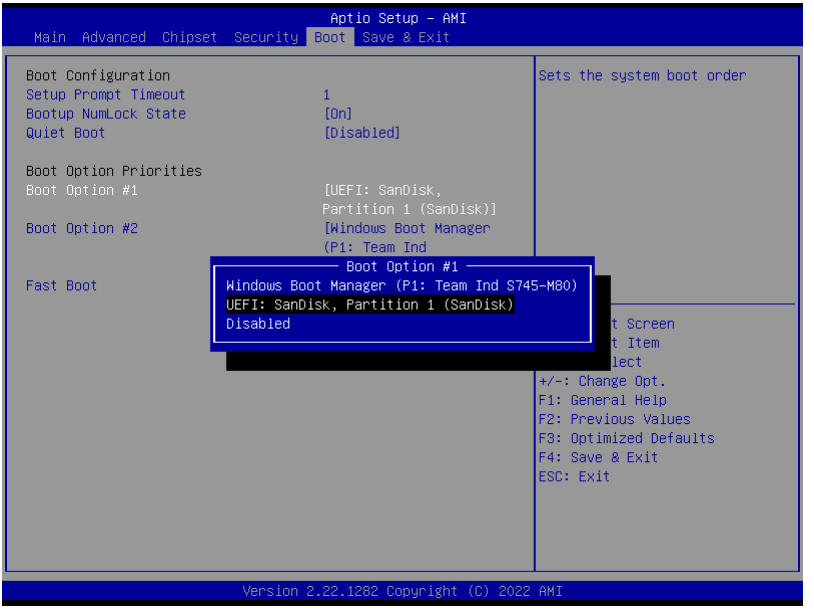
4 Make sure the target system can first boot to the bootable device.

(1) Connect the bootable USB device.

(2) Turn on the computer and press <**ESC**> or <**DEL**> key during boot to enter BIOS Setup.

(3) Select [**Boot**] menu and set the USB bootable device to be the 1st boot device.

(4) Press <**F4**> to save the configuration and exit the BIOS setup menu.



II. AFUEFIx64 Command for System BIOS Update

AFUEFIx64.efi is the AMI firmware update utility; the command line is shown as below:

AFUEFIx64 <ROM File Name> [option1] [option2]….
Users can type "AFUEFIx64 /?" to view the definition of each control option. The recommended options for BIOS ROM update include the following parameters:

/P: Program main BIOS image.
/B: Program Boot Block.
/N: Program NVRAM.
/X: Don't check ROM ID.

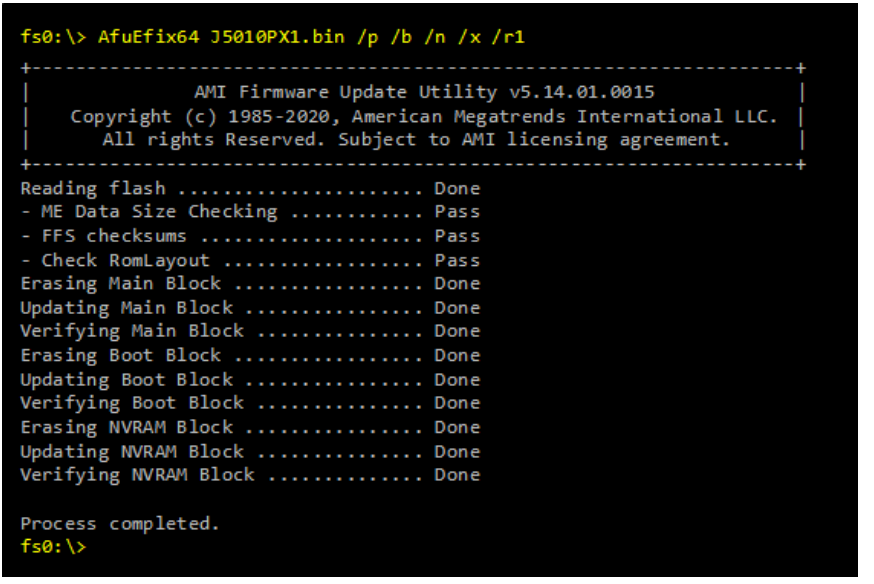
III. BIOS Update Procedure

1 Use the bootable USB storage to boot up system into the EFI Shell.

2 Type "**AfuEfix64 J501xxxx.bin /p /b /n /x /r1"** and press Enter to start the flash procedure. (xxxx means the BIOS revision part, e.g. 0PM1…)

3 During the update procedure, you will see the BIOS update process status and its execution percentage. Beware! Do not turn off the system power or reset your computer if the whole procedure are not complete yet, or it may crash the BIOS ROM and the system will be unable to boot up next time.

4 After the BIOS update procedure is completed, the following messages will be shown:



5 Restart the system and boot up with the new BIOS configurations.

6 The BIOS Update is completed after the system is restarted.

7 Reboot the system and verify if the BIOS version shown on the initialization screen has been updated.